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Investigation of CNTFET Performance with Drain Control Coefficient Effect

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Abstract A deep study on the effects of drain control coefficient (α_D) on the performance of Carbon Nanotube Field Effect Transistor (CNTFET) has been conducted in this work. In this research, a new analytical CNTFET simulation along with a MATLAB multiple parameter approach model with 3D output has been employed to examine the device performance. It is found that- drain current, drain conductance and transconductance increase with high drain control coefficient causing the device to perform better. However, DIBL also increases with α_D resulting in degraded performance of the device. In addition, subthreshold swing moves away from the ideal value as α_D goes up which is also not desired for low threshold voltage and low-power operation of scaled down FETs.

Keywords Drain Control Coefficient (α_D), CNTFET, Drain Current, Transconductance

1. Introduction

The existing Silicon technology is struggling to keep up with the demands of Moore's Law and International Technology Roadmap for Semiconductors (ITRS) **[1]**. Carbon Nanotube (CNT), since its invention by S. Iijima **[2]**, has aroused the curiosity of researchers from the world over for FET applications because of its excellent mechanical **[3]** and electrical properties **[4]**, **[5]**. The performance of CNTFET under different conditions have already been analysed and reported by a number of researchers in recent years **[6-18]**. Previously, the effect of dielectric constant (K), gate oxide thickness, temperature, chirality and gate control coefficient on the performance of Carbon Nanotube Field Effect Transistor (CNTFET) has been studied by *Khan et al.* **[6-10]**, **[19]** with a three dimensional multiple parameter simulation model. It has been found that I_{ON}/ I_{OFF}, transconductance and average velocity carrier goes up with high K and so, the on-state current of the CNTFET goes up. At the same time, the subthreshold swing also rises with the rise of the value of K. Scientists have observed that the on current maintains an inverse relationship with the gate oxide thickness **[7], [10], [13], [20], [21]**. Traditional MOSFET (Metal Oxide Semiconductor Field Effect Transistor) suffers from channel scattering, tunneling and various other problems when the gate oxide thickness enters the nanometer regime **[20]**. Carbon nanotubes are not plagued by such problems as all chemical bonds are satisfied in a carbon nanotube and thus, there is less oxide to channel interface problem. A multitude of oxide can be placed on the nanotube and thus, many high-k dielectrics can be incorporated into CNTFET to reduce the tunneling current. Also, a higher I_{ON}/I_{OFF} has been reported in lower gate thickness than in higher gate thickness **[7], [20]**. Furthermore, the effect of temperature on the operation of CNTFET has been investigated and it has been concluded that temperature wields a negligible influence on the performance of CNT transistor **[8]**. Drain control coefficient (α_D) is an important parameter while modelling CNTFET and analysing its performance in both ballistic and non-ballistic regime. Hence, it is very crucial to investigate how CNTFET performance depends on α_D. This investigation will also help scientist to perform efficient and optimum CNTFET device fabrication. Hence, this paper endeavours to study the impact of Drain Control Coefficient (α_D) on the performance of CNTFET.

The experiment has been carried out by analysing the change in current-voltage (I-V) characteristics, transconductance, drain conductance, subthreshold swing and drain induced barrier lowering (DIBL) effect with developed multiple simulation method.

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2. CNTFET Structure and Simulation Model

A MOSFET-like CNTFET has been considered for the purpose of this experiment. The drain and source terminals of the considered FET are heavily doped similar to the conventional MOSFET. This device is designed to overcome the problems faced by SB-CNTFET by operating like a simple MOSFET. The barrier height in this FET is modulated by gate voltage. Charge induced in the channel by the gate terminal controls the drain current **[22-24]**.

CNTFET is able to suppress ambipolar conduction. At the same time, it provides longer channel length limit as the density of metal-induced-gap-states are significantly reduced. As the length between gate and source/drain terminals can be separated by the length of source to drain, parasitic capacitance and transistor delay metric can be reduced and hence, operating speed of the device can be increased. It has already been shown **[21]** that CNTFET provides higher on-current compared to SB-CNFET as its operating principle is similar to that of SB-CNFET with negative Schottky barrier height during on-state condition and so the upper limit of CNTFET performance can be justified.

A three dimensional multiple simulation tool **[25]** was developed based on ballistic nanotransistors theory **[22]** and FETToy tool **[26]**. The flow diagram of the simulation model is depicted in **APPENDIX [19]** and code has been developed using MATLAB program. The detailed simulation process has been discussed in our earlier publication **[25]**. In this modeling, there are several options for choosing particular parameter to observe the effect of CNTFET output while others set as default value. That is the reason of naming it 'Multiple simulators'. The total simulation is divided into three parts:

A. Command Window
B. Physical Calculation
C. Final output

Command window is subdivided into three segments named: Parameter choosing, Deciding range and finally iteration. 'Command Window' is the core part to decide the parameters. This research has considered six parameters to observe the CNTFET attributes. In this fragment, researchers have to decide the logical maximum and minimum value for specific parameters. Consequently, the iteration will start according to the range decided by researcher up to maximum value. In addition, if no other parameters are changed than the simulator will go for default value which is set by us.

According to the decided parameter and value, simulator starts physical calculation. It takes each value from the range, calculates nine steps of the physical calculation and repeats same patterns for other values also. It calculates until gaining final result for the final values. Immediately after the entire calculation, it sends values to output window for making 3D output.

The analysis starts at the top of the energy barrier since current remains the same throughout the channel and all scattering mechanism is neglected. At any specified drain/gate voltage, the drain current is calculated based on the total charge that occupied first subband in the nanotube. The process is repeated for all drain/gate voltage in the specified range before all the drain current values are plotted within a single graph. The model for ballistic CNFET consists of three capacitors, which represents three transistor terminals on potentials at top of barrier. The mobile charge is determined by the local density of states at top of the barrier, location of source and drain levels, E_{F1} and E_{F2}, and self-consistent potential at top of the barrier, U_{scf}. Steps of calculating the drain current **[22]**:

1. Consider a value of V_g, V_{ds}, V_s and E_{F1}. For simplicity, V_s is grounded as potential reference.
2. Compute the total charge on nanotube channel. The charge at top of the barrier contributed from source and drain are given as

$$N_1 = D(E)/2 \int_{-\infty}^{\infty} f(E + U_{scf} - E_{F1})dE \quad (1)$$

$$N_2 = D(E)/2 \int_{-\infty}^{\infty} f(E + U_{scf} - E_{F2})dE \quad (2)$$

Where, N_1 represents positive velocity states filled by source and N_2 represents negative velocity states filling by drain, $E_{F1(F2)}$ is the source (drain) Fermi level, f(E) is the probability that a state with energy E is occupied (Fermi-Dirac probability), D(E) is the nanotube density of states (DOS) at top of the barrier and U_{scf} is self-consistent potential at the top of the barrier. For simplicity, assume source Fermi level as the reference, thus $E_{F1} = 0$ and $E_{F2} = -qV_{DS}$ where q is electronic charge.

3. U_{scf} must be evaluated in order to solve for charge density at top of the barrier. U_{scf} can be solved by using superposition. First, Laplace potential is calculated using the following equation:

$$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) \quad (3)$$

Where,

$$\alpha_G = C_G/C_\Sigma,\ \alpha_D = C_D/C_\Sigma,\ \alpha_S = C_S/C_\Sigma \quad (4)$$

Now, potential due to mobile charge calculated as

$$U_p = q^2/C_\Sigma (N_1 + N_2) - N_0 \quad (5)$$

Where,

$$N_0 = \int_{-\infty}^{\infty} D(E)f(E - E_F)dE \quad (6)$$

Now, U_{scf} can be found by adding U_L and U_P:

$$U_{scf} = U_L + U_p$$
$$= -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + q^2/C_\Sigma (N_1 + N_2) - N_0 \quad (7)$$

4. Now, Drain current can be computed by using following formula:

$$I_D = 4qk_BT/h\ [\ln(1+\exp(E_{F1}-U_{scf})) - \ln(1+\exp(E_{F2}-U_{scf}))] \quad (8)$$

Where, k_B is Boltzmann constant, T is operating temperature and h is Planck's constant.

5. By repeating step (i)-(iv) for a set of (V_G, V_D) points, the I_D (V_G, V_D) characteristics can be determined.

3. Results and Discussions

For the purpose of this research, a (13,0) CNT was considered which had a bandgap of ~0.83 eV and a diameter of ~1.0184 nm. A coaxial gate, separated by a 1.5 nm thick oxide, was placed around the intrinsic part of the nanotube. For this observation, the temperature was kept constant at 300 K and the gate control coefficient (α_G) was set at 0.88. In addition, the source Fermi level was -0.32 and the value of dielectric constant was 3.9.

Figure 1 shows the I-V characteristics of CNTFET with respect to drain control coefficient. The drain control parameter was varied from 0.025 to 0.225 at an interval of 0.01. From the figure it is evident that the drain current gradually increases with the increase of drain control coefficient and maintains the trend until it reaches 0.225. This substantiates the claim that drain control coefficient and drain current maintains a proportional relationship **[27]**.

One of the key parameters of scaling of transistors is the subthreshold swing. A small subthreshold swing (S) is necessary for maintaining a satisfactory value of I_{on}/I_{off}. Also, to get a low threshold voltage and to operate FETs which have been scaled down to small sizes at low-power, a low value of subthreshold swing is advantageous. Theoretically, the lowest possible value for S is, $S= (K_BT/e)\ \ln(10) =$ 60mV/decade at room temperature **[18]**. **Figure 2** shows that the after remaining stable for the interval of ~0.02 to ~0.06, then the swing starts to increase and keeps increasing until ~0.2. There is a slight fluctuation between ~0.2 and ~0.25. This observation indicates that lower drain control coefficient is desirable in order to have better CNTFET response.

The DIBL effect is a short channel effect which can change the channel from a state of pinch-off to conduction. This results in a substantial leakage current. It also affects the threshold voltage and makes the gate ineffective in controlling the channel. As a result, the DIBL effect debases the device performance and this should be avoided while designing the circuit **[23]**.

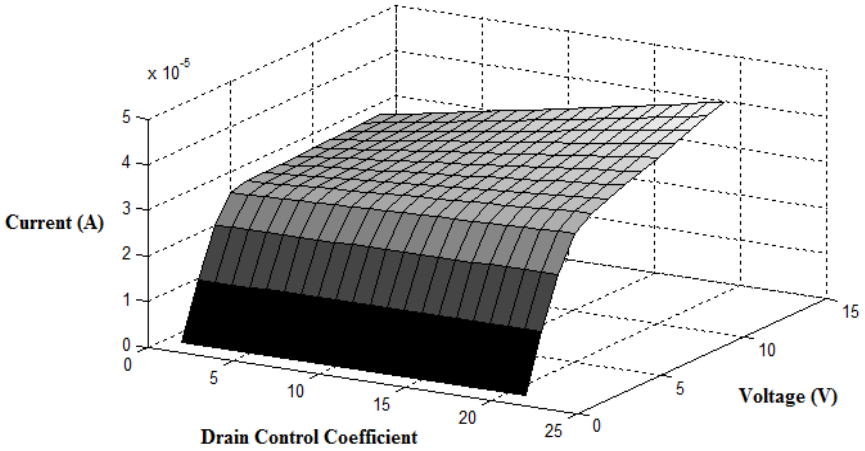

Figure 1. Current-Voltage output with respect to Drain Control Coefficient

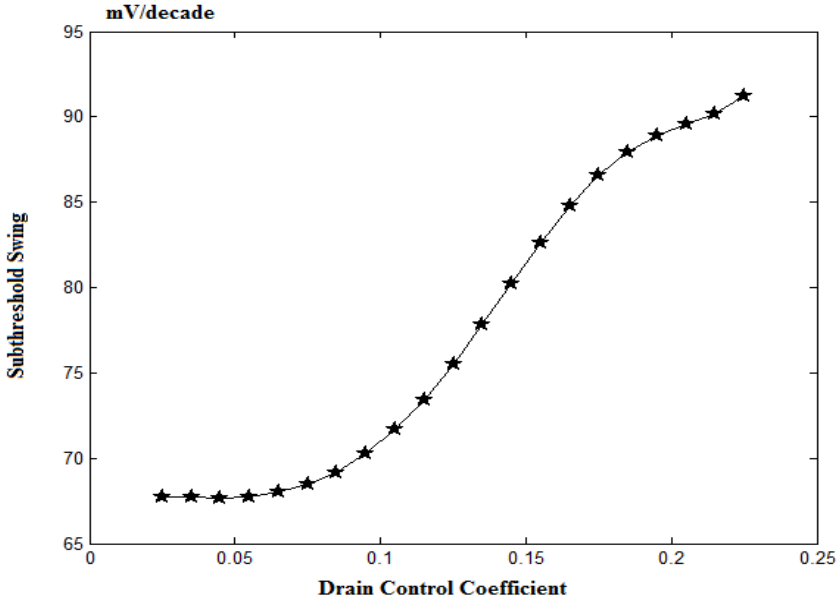

Figure 2. Subthreshold swing as a function of Gate Control Coefficient

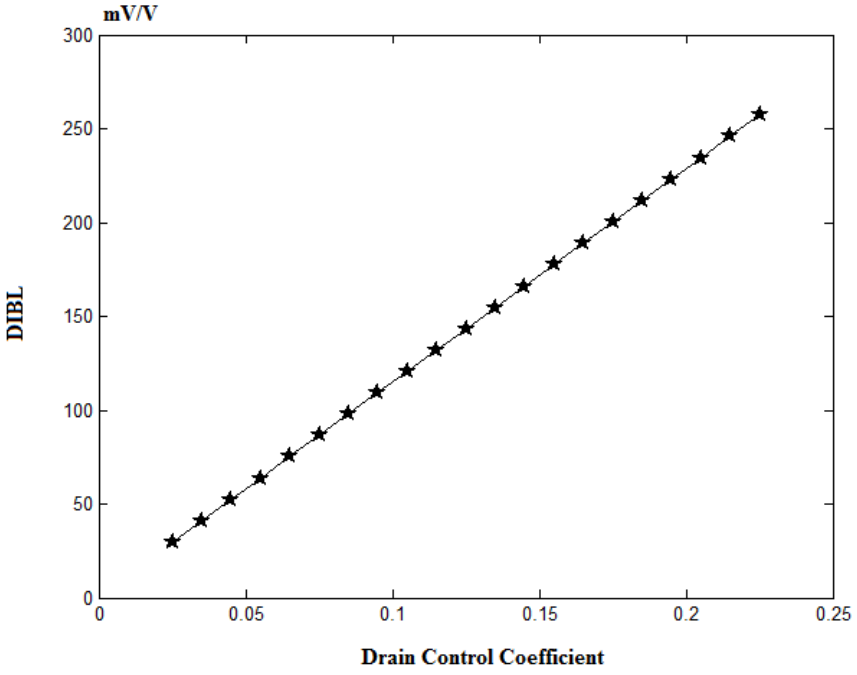

Figure 3. DIBL effect with Drain Control Coefficient

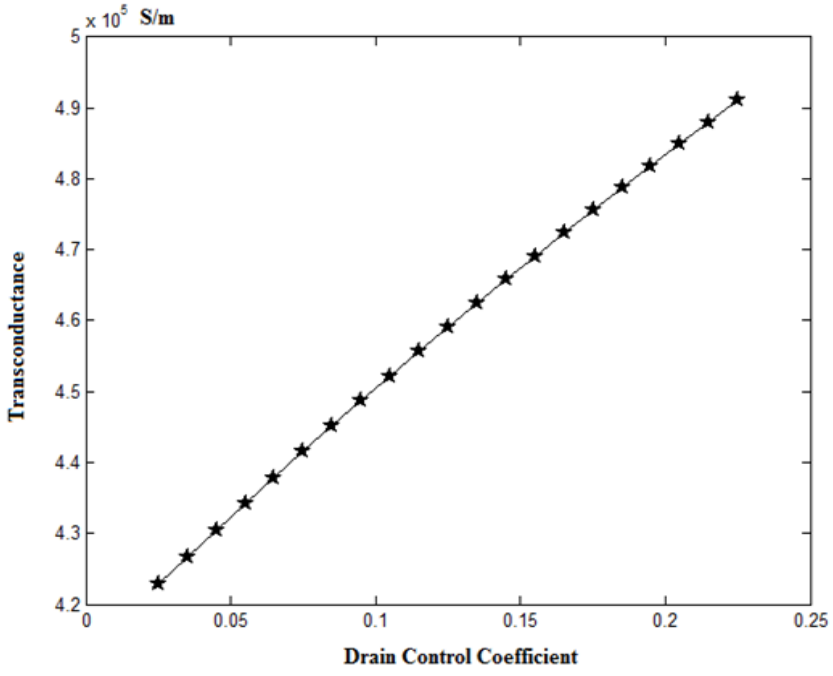

Figure 4. Transconductance as a function of Gate Control Coefficient

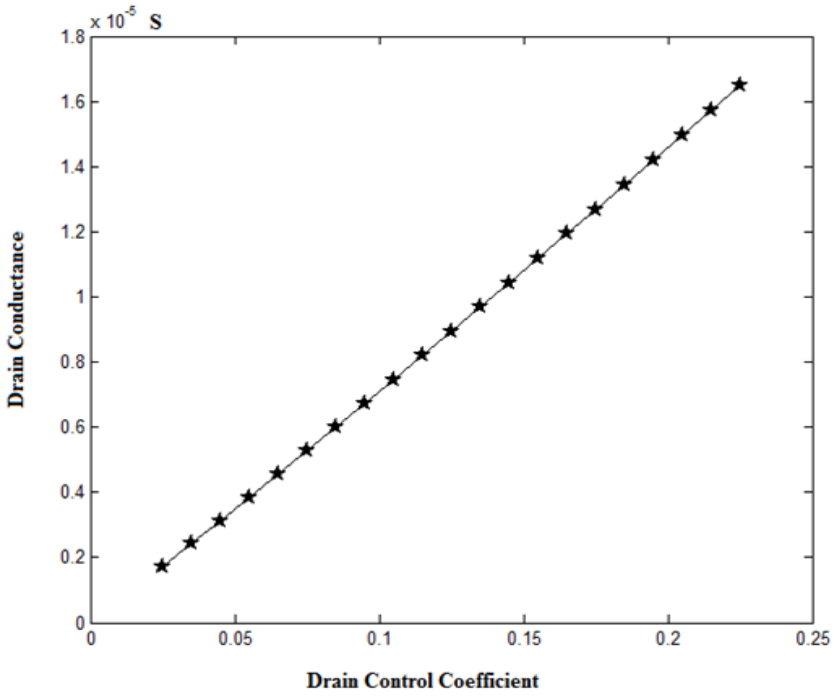

Figure 5. Drain conductance as a function of Drain Control Coefficient

DIBL effect occurs when the barrier height for channel carriers at the edge of the source goes down because of the influence of the drain electric field. From **Figure 3**, it can be seen that DIBL increases almost linearly with the drain control coefficient and so, this is not desirable. Therefore, CNTFET will perform more like an ideal device if the drain control coefficient is kept low.

Figure 4 is extracted from the slope of I_D-V_{GS} and depicts the relationship between transconductance and drain control coefficient. It can be seen from the plot that transconductance of the considered CNTFET increases with α_D. It can be deduced from this that I_{on}/I_{off} increases with the increase of α_D which ultimately leads to higher on-state current and at the same time, maintains the leakage current level. According to the Sanudin et al. **[27]** leakage current increases exponentially when the coefficient is greater than 0.08. **Figure 5** presents the relationship between α_D and drain conductance and it can be easily seen that the drain conductance rises almost linearly with the drain control coefficient.

4. Conclusions

In this work, the effect of drain control coefficient on ballistic CNTFET is analyzed with an iterative 3D multiple simulation method. It can be concluded from the results that a high α_D causes the device to respond slower. Also, α_D increases the leakage current and degrades the CNTFET output. Furthermore, the subthreshold swing moves away from the theoretical value as α_D goes higher. However, transconductance and drain conductance increases with drain control coefficient. To sum up, a lower value of drain control coefficient (α_D) is more desirable for better CNTFET performance.

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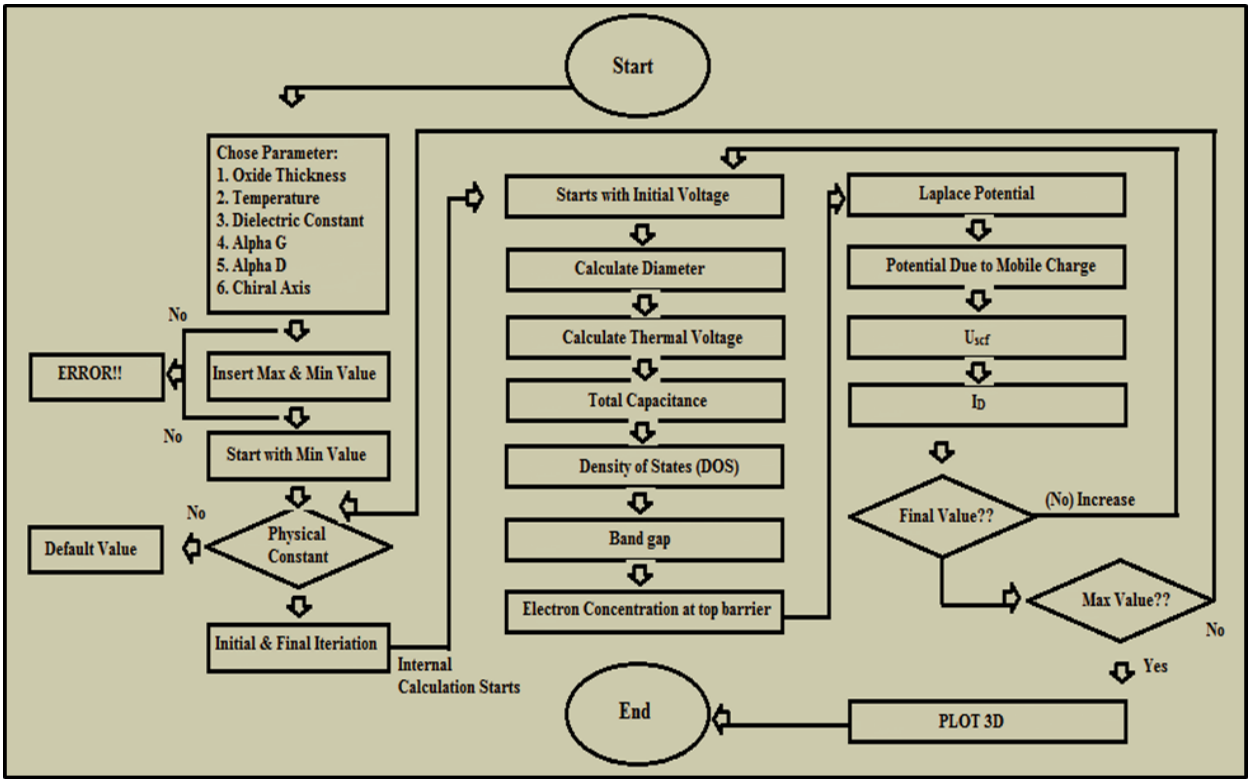
Nomenclature

α_D	drain control coefficient
K	dielectric constant
I_{ON}	drain current during on state
I_{OFF}	drain current during off state
I-V	current-voltage characteristics
α_G	gate control coefficient
S	subthreshold swing
K_B	Boltzmann's constant
T	temperature
I_D	drain current
V_{GS}	gate-source voltage

Appendix

Flow diagram of the multiple parameter approach simulation tool



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