

A Continuous-Time Sigma-Delta Modulator with a Hybrid Loop Filter and Capacitive Feedforward

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Abstract A continuous-time (CT) sigma-delta ($\Sigma\Delta$) modulator clocked at 128 MHz with a hybrid active-passive loop filter is presented for WCDMA applications. The proposed 5th-order loop filter architecture mainly consists of two passive integrators and three active integrators. To erase the summation amplifier used in the chain of integrators with weighted feedforward summation (CIFI) topology, the capacitive feedforward structure is employed. In addition, local feedback resistors form the bridge-T network to reduce the chip area. The prototype chip is fabricated with TSMC 0.18 μm CMOS technology. Under the supply voltage of 1.8 V, measured results have achieved the best FOM of 2.67 pJ/conv, a dynamic range of 62 dB, a SNDR of 60.26 dB, an ENOB of 9.72 bit, IM3 of -48 dB and a power consumption of 9 mW over a 2 MHz signal bandwidth. Including pads, the chip area is 0.642 (1.07 x 0.6) mm².

Keywords Sigma-Delta Modulator, $\Sigma\Delta$ Modulator, WCDMA, CIFI

1. Introduction

With increasing development of wireless communication systems, there is a large demand in the wireless communication for analog-to-digital converters (ADCs) that require signal bandwidths of several mega-hertz. Sigma-delta modulators are ideally suitable for such applications. Compared to the discrete-time switched capacitor circuit implementations, CT $\Sigma\Delta$ modulators have the potentials for wider bandwidth and are also inherent anti-aliasing.

Most of the designed loop filters of CT $\Sigma\Delta$ modulators are the combination of active-RC and/or Gm-C integrators because the amplifiers of the active integrators can provide higher gain, which will greatly make input-referred noise be reduced. However, they consume power, and the amplifier design in low voltage application is also challenging. Several literatures of $\Sigma\Delta$ modulators with passive loop filter are easily to find [1]. These modulators are simple compared to active counterparts as well as introduce less distortion and consume no power. However, high order passive filters by cascading are difficult to implement because of loading effect. As a result, in order to reach higher resolution, passive $\Sigma\Delta$ modulators usually require large oversampling ratio (OSR).

The CT $\Sigma\Delta$ modulators with hybrid active-passive loop

filters are considered to combine the merits of both active and passive filters. Literature [2] proposed a 5th-order CT $\Sigma\Delta$ modulator, and its active integrators are placed on the first, third, and fifth stages of the loop filter. The second and fourth integrators are realized as passive networks. This hybrid arrangement reduces power consumption compared to all active counterparts. Although placing passive integrators on second and fourth stages of the loop filter mitigates the loading effect, the noises referred to input stage are only suppressed by one and two active integrators respectively. The literature [3] proposes a hybrid loop filter using single amplifier biquad (SAB). However, there is no information about the required gain and bandwidth of the amplifier of the mentioned SAB.

It is well-known that higher-order loop filter can achieve good resolution, but its structure becomes complicate and consumes much power. In contrast to the higher-order loop filter, the lower-order loop filter is simple, but it accounts for bad resolution. Hence, considering those factors, in this paper, we extend and improve our previous result reported in 2011 Midwest symposium; a hybrid 5th-order single-bit CT $\Sigma\Delta$ modulator with a hybrid active-passive loop filter is presented [4]. Passive filters are placed on third and fifth stages of the loop filter to mitigate their noise contribution. Small signal gain which suppresses in-band noise is provided by active-RC integrators. Also, the capacitive feedforward is adopted to erase a summation amplifier used in CIFI topology. Local feedback inside loop filter can improve SNDR (signal-to-noise-and-distortion ratio) but usually occupies more layout area. The bridge-T network is designed to alleviate this issue.

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The rest of the paper is organized as follows. In Section II, the proposed CT $\Sigma\Delta$ modulator with a hybrid active-passive loop filter and its design procedure are presented. In Section III, clock jitter is discussed. Measured results are given in Section IV. Finally, conclusion is made in section V.

2. The Proposed CT $\Sigma\Delta$ Modulator with a Hybrid Active-Passive Loop Filter

2.1. The Proposed $\Sigma\Delta$ Modulator Architecture

Figure 1 depicts the architecture and clock timing of the proposed CT $\Sigma\Delta$ modulator. The proposed CT $\Sigma\Delta$ modulator circuit is shown in Figure 2. The first two stages of the loop filter are active-RC integrators where C_1 in series with R_z is to cancel the right-half-plane zero due to the excess loop delay[5]. Passive networks are placed on third and fifth stages of the loop filter. The noises referred to input are therefore suppressed by at least two active integrators. Compared to the prior art, such arrangement can further mitigate the input noise contribution of passive filters.

stages of the loop filter. The transfer function of the hybrid loop filter can be expressed as:

$$H(s) = \frac{a_1}{s} \cdot b + \left[\left(\left(\frac{a_2}{s} + k_2 \right) \cdot \frac{k_3 + a_3/s}{1 + a_3/s} + k_1 \right) \cdot \frac{a_4}{s} \right]^{-1} \cdot \frac{k_4 + a_5/s}{1 + a_5/s} \quad (1)$$

Coefficient values in (1) are readily obtained from running Matlab Toolbox and they are $a_1=0.5$, $a_2=0.3$, $a_3=0.13$, $a_4=0.39$, $a_5=0.13$, $k_1=1.34$, $k_2=1.2$, $k_3=0.67$, $k_4=0.67$, and $b_1=0.087$.

The proposed CT $\Sigma\Delta$ modulator circuit is shown in Figure 2. Obviously, the first two stages of the loop filter are active-RC integrators where C_1 in series with R_z is to cancel the right-half-plane zero due to the excess loop delay[5]. Passive networks are placed on third and fifth stages of the loop filter. The noises referred to input are therefore suppressed by at least two active integrators. Compared to the prior art, such arrangement can further mitigate the input noise contribution of passive filters.

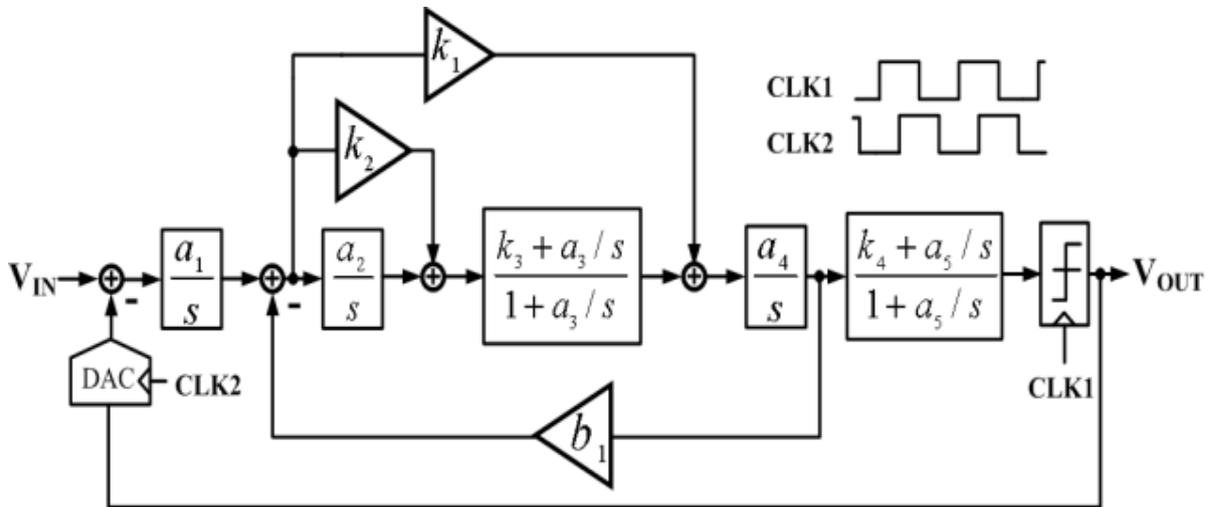


Figure 1. The architecture of the proposed CT $\Sigma\Delta$ modulator

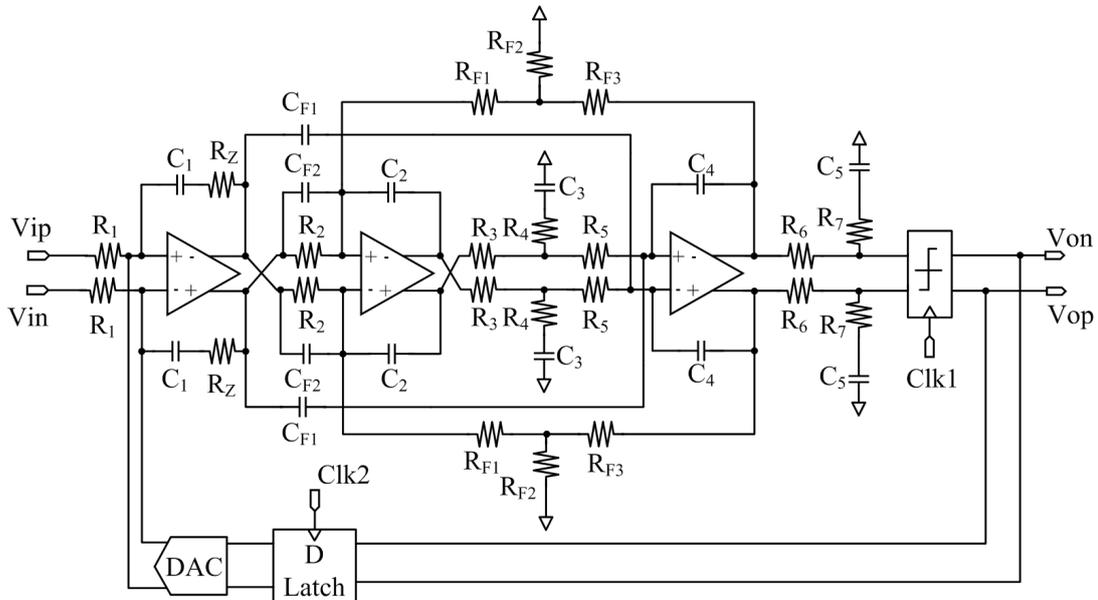


Figure 2. The proposed CT $\Sigma\Delta$ modulator with a hybrid active-passive loop filter

2.2. Passive Filter Circuit

The schematic of the passive filter is shown in Figure 3, and the corresponding transfer function is expressed as:

$$H(s) = \frac{V_o}{V_i} = \frac{1 + s(R_2 C_1)}{1 + s(R_1 + R_2)C_1}. \quad (2)$$

The passive filter is a lossy device with one pole at $1/(R_1 + R_2)C_1$ and one zero at $1/R_2 C_1$. Since the DC gain is always less than one, the output noise of the passive filter can be directly referred to the input.

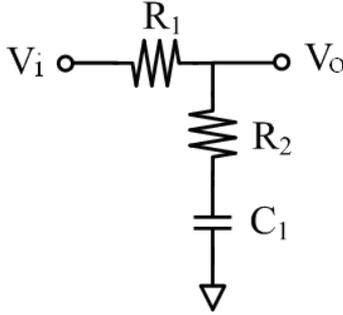


Figure 3. A passive filter circuit

2.3. Active Bridge-T Network

Considering the design of the hybrid loop filter, an optimization theory for the passive loop filter based on the trade-off of both circuit noise and noise transfer function is discussed in[3]. However, no optimization theory about poles and zeros of the hybrid loop filter is found. Therefore, the active 3rd order loop filter is first designed with Delta-Sigma Toolbox. The design of poles and zeros of the two passive filters is based on the locations of poles and zeros of the 3rd-order active filter. After embedding the two 1st-order passive filters into the active 3rd-order filter, the dynamic range scaling methodology of the 5th-order hybrid loop filter is performed to ensure op amps are not saturated due to the larger signal swing. This is verified by scaling (increasing or decreasing) the coefficient values of the hybrid loop filter while maintaining its transfer function as identical as possible.

The order design of the hybrid loop filter is based on following principles. First, cascading several stages of passive filters should be avoided because of loading effect, attenuation and noise accumulation. Secondly, the active integrators should be preceded passive filters wherever possible since the gain of passive filter is less than one. Although the noise of passive filters can be mitigated with parallel larger capacitance and series smaller resistance, it demands preceded stage with higher driving capability, and hence more power dissipation and consume much chip area due to large capacitance.

The local feedback inside loop filters can increase modulator SNDR, but this structure will require more chip area and will cause more cost. The bridge-T network shown in Figure 4 can effectively mitigate this issue.

The transfer function of the bridge-T network is:

$$\frac{V_o}{V_i} = \frac{R_2}{R_1} \times (2 + k). \quad (3)$$

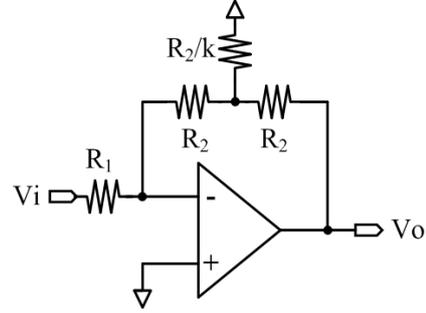


Figure 4. An active bridge-T network

The bridge-T network achieves an effective feedback resistor of $R_2(k+2)$. If the feedback resistor R_2 is 40 kΩ and k is set to be approximate 5.5, then the equivalent resistance becomes 300 kΩ. This result highly reduces the chip area of feedback resistors by a factor of three times.

The fifth order $\Sigma\Delta$ modulator is stabilized by the resistive feedforward $\{R_4/(R_3+R_4), R_7/(R_6+R_7)\}$, and the capacitive feedforward $(C_{F2}/C_2, C_{F1}/C_4)$. The former structure is that in the higher frequency, C_3 and C_5 are short so that the feedforward paths are formed[3]. Capacitive feedforward is a simple solution compared to conventional CIFF topology[6]. Instead summing all feedforward paths by an extra summation amplifier, which usually demands high slew rate, two capacitive feedforward paths are disturbed by two op amps inside the loop filter.

2.4. Tunable Capacitor Array

Since the resistance variation of R due to the process actually is evident, sometimes the error may highly reach about $\pm 30\%$. To compensate this large RC product variation, capacitors are implemented as capacitor arrays as shown in Figure 5. The nominal value of the capacitor array is equal to $5C$, as $(b_2, b_1, b_0) = (0, 1, 0)$. The capacitor array is tunable from $3C$ to $10C$, corresponding 60% to 200% of the nominal value. The reset switch protects the device returning the modulator to a safe state in case of overload.

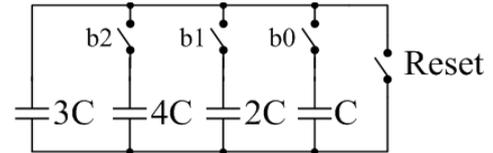


Figure 5. A tunable capacitor array

2.5. Operational Amplifier Design

The load capacitance of each amplifier is similar due to deliberate design. The two-stage amplifier is used, shown in Figure 6 which is a two-stage that consists of a differential input stage, a common source output stage with a frequency compensation circuit of C_c in series of R_1 and a common-mode feedback (CMFB). The CMFB circuit has advantages of allowing rail-to-rail output swing. Furthermore, it does not need any level shift or attenuation on the common mode signal, unlike other CMFB circuits

that use differential pairs. The required gain and bandwidth of the amplifier are determined by simulation. Simulated results illustrate that the op amp achieves a unity gain bandwidth (GBW) more than 350 MHz parallel with a load capacitance of 3 pF and a phase margin of 64°. The low-frequency gain of the op amp is higher than 50 dB at 1.8 V supply voltage. All other performances are summarized in Table 1.

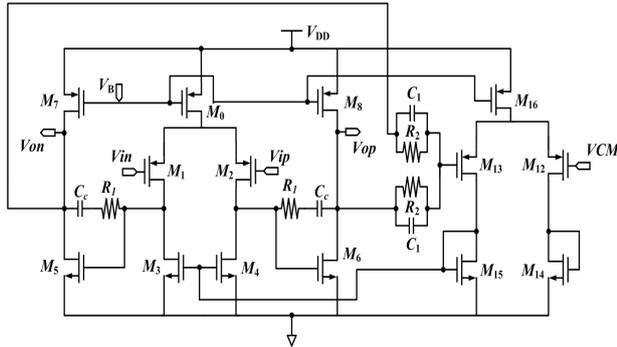


Figure 6. A two-stage amplifier with common mode feedback circuit

Table 1. Op Amp Performance Summary with an Output Load of 3 pF/25 kΩ

Parameters	Spec.	Pre-Sim.	Post-Sim.
Output Load	-	3 pF // 25 k	□
DC Gain	> 50 dB	58.76 dB	58.8 dB
Phase Margin	> 60°	67.9°	64.3°
Unity Gain	>350	430 MHz	422 MHz
Bandwidth	MHz		
Offset Voltage	-	-	0.1 mV
Setting Time + (1%)	< 3.9 ns	1.5 ns	1.6 ns
Setting Time - (1%)	< 3.9 ns	0.8 ns	1 ns
Slew Rate +	-	155.4 V/μs	126.9 V/μs
Slew Rate -	-	219.6 V/μs	159.5 V/μs
ICMR	-	0.23V~1 V	0.24V~1 V
OCMR	> 1V	0.18V~1.48V	0.19~1.48V
PSRR +	> 60dB	-	84 dB
PSRR-	> 60dB	-	82.8 dB
CMRR	> 60dB	-	78.6 dB
THD @ 1 Vp-p, 1 MHz Input	< 1%	0.37 %	0.39 %
Power	< 5mW	2.88 mW	2.67 mW
Consumption			
Input-Referred Noise	-	13.34 uVrms	16.69 uVrms
Layout Area	-	-	163 x 100 μm ²

2.6. Bias with a Start-Up Circuit

The bias circuit used for the proposed modulator is shown in Figure 7. The I_{out} given in (4) is tunable by varying off-chip resistor R_B and is independent of the power supply, $k = \mu_n C_{ox}$ is called the process conduction parameter. The bias circuit requires a start-up circuit to avoid $I_{out}=0$. When the gate voltage of M_{B4} and M_{B5} is zero, M_{B7} is turned on to initialize the current. After M_{B5} and M_{B4} are turned on, M_{B7} biased by M_{B3} and M_{B6} is turned off immediately.

$$I_{out} = \frac{2}{\mu_n C_{ox} (W/L)_N} \cdot \frac{1}{R_B^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2. \quad (4)$$

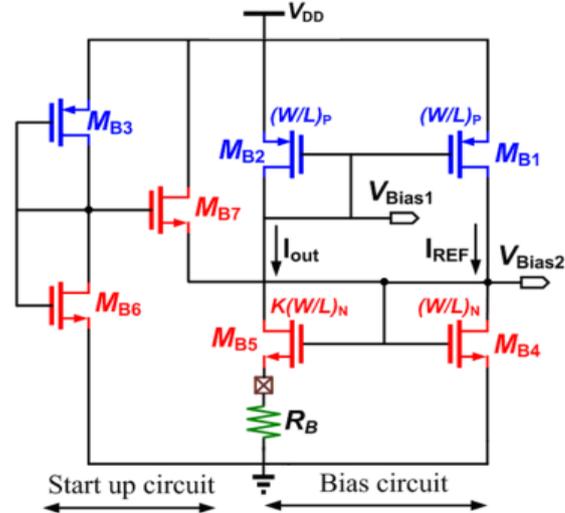


Figure 7. The bias with a start-up circuit

2.7. Quantizer, D-Latch, and Feedback DAC

Dynamic comparator circuit with SR (set reset) latch is chosen for low power consumption, as shown in Figure 8. Simulation verifies that the regeneration time is 1.5 ns, the offset voltage is less than 10 mV and the power consumption is less than 20 μW. Both the comparator and the D-latch in Figure 8 use the same clock frequency of 128 MHz.

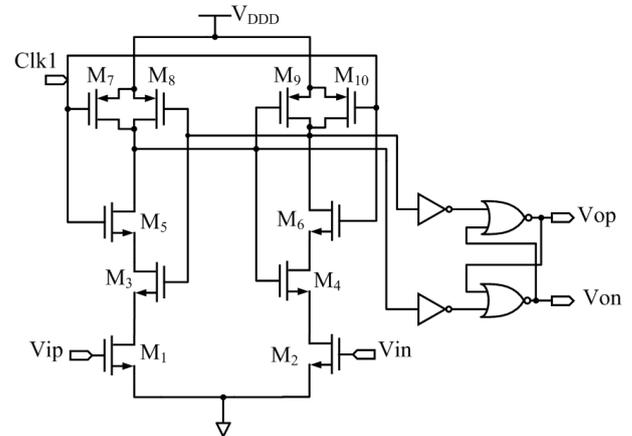


Figure 8. Dynamic comparator with SR latch

But to allocate sufficient regeneration time to the comparator, the D-latch has to be delayed for approximately one-fourth clock cycle. This arrangement greatly reduces harmonic distortion. The D-latch circuit is shown in Figure 9.

A complementary current steering DAC with nonreturn-to-zero (NRZ) pulse is adopted, as shown in Figure 10. This circuit is less sensitive to clock jitter compared to return-to-zero (RZ) and half return-to-zero (HRZ) implementation.

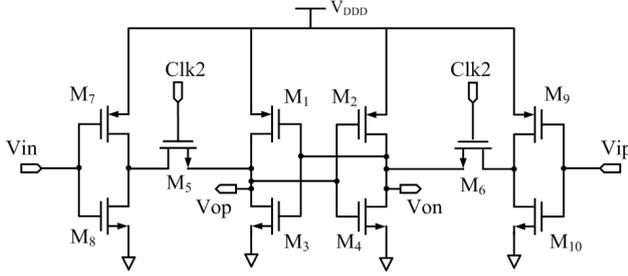


Figure 9. A D-latch circuit

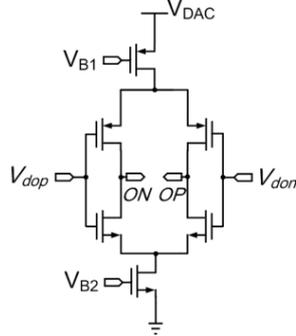
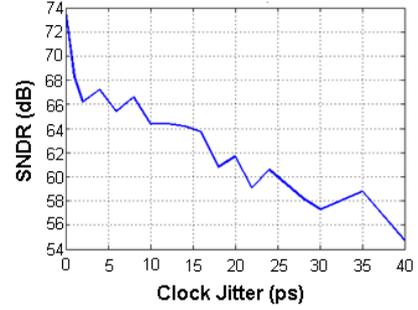


Figure 10. A DAC circuit

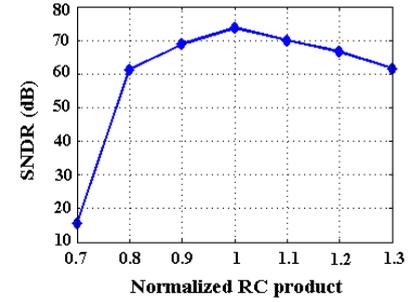
3. Clock Jitter

Jitter is the undesired deviation often from a reference clock source and may lead to data errors. If there is jitter present on the clock signal to the ADC or DAC then the instantaneous signal error will be introduced. Usually, it is a significant and undesired factor in almost all communications links and can cause loss of transmitted data between ADC or DAC. The amount of tolerable jitter depends on the affected application. A CT $\Sigma\Delta$ modulator is sensitive to the DAC output over the entire feedback period, unlike a discrete-time implementation which relies only on the final settled output value. The DAC timing jitter corrupts the output of the feedback pulse and is often the main error source in high resolution CT $\Sigma\Delta$ modulator[9]. A filter followed can be designed to minimize the effect of sampling jitter. The output of the first feedback DAC is especially critical. CT $\Sigma\Delta$ modulators are also sensitive to clock jitter. In order to quantify the effects of the clock jitter, the modulator was simulated with a normally distributed jittered clock signal. Figure 11(a) depicts the SNDR of the modulator versus clock jitter.

To maintain SNDR large than 60 dB, the RMS value of clock jitter must less than 22 ps at the clock rate of 128 MHz. To reduce the sensitivity of clock jitter for CT $\Delta\Sigma$ modulator, SCR feedback is introduced[10]. It could be employed to the single-bit hybrid $\Delta\Sigma$ modulator coefficient deviation of loop filter of CT $\Sigma\Delta$ modulators and is a common issue due to RC product variation, which is about $\pm 30\%$. Figure 11(b) depicts the modulator SNDR versus the normalized RC product. Obviously, at normalized RC=1, the SNDR is maximum.



(a)



(b)

Figure 11. Simulated SNDR values versus (a) clock jitter and (b) normalized RC product

4. Measured Results

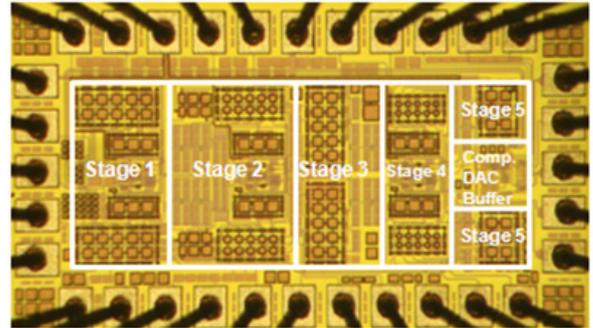


Figure 12. Chip microphotograph of the proposed $\Sigma\Delta$ modulator with a chip area of 0.642 (1.07x0.6) mm²

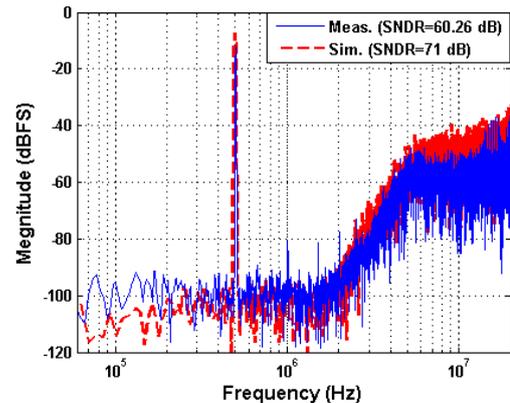


Figure 13. Output spectrum (input signal: 0 dBm, 500 kHz)

The proposed prototype chip microphotograph is shown in Figure 12. A balun device in this measurement is selected to convert the single-ended analog signal to a balanced quadrature-differential signal. Notably, op amps often consume the most area. Comparator, DAC and buffer circuits take a small chip. Figure 13 shows the measured output spectrum of the modulator at a sampling rate of 128 MSamples/s. A 0 dBm 500 kHz input sinusoid was used. The measured output stream is loaded into MATLAB and taken 16384 points FFT with Hanning window in order to estimate the SFDR, SNDR, image rejection (IR) and input dynamic range (DR). The measured results of output spectrum accompanying with the simulated results are almost the same shown in Figure 13. The measured peak SNDR is 60.26 dB over a 2 MHz signal bandwidth. Figure 14 shows the measured IM3 to be -48 dB. The SNDR versus input signal level is plotted in Figure 15, showing that the measured dynamic range is 62 dB.

Comparison to other reported $\Sigma\Delta$ modulators can be carried out by evaluating the figure-of-merit (FOM)[9]:

$$\text{FOM} = \frac{P_{\text{diss}}}{2 \times \text{Bandwidth} \times 2^{\text{ENOB}}}, \quad (5)$$

where P_{diss} is the power consumption in mW and the bandwidth is in Hz.

Table 2 summarizes the measured performance of the proposed $\Sigma\Delta$ modulator in comparison with some recently reported $\Sigma\Delta$ modulator papers. Based on this comparison table, the proposed hybrid $\Sigma\Delta$ modulator achieves a FOM=2.67 pJ/step within a 2.0 MHz bandwidth, and consumes only 9 mW of power. Literatures[8, 9] accompany the bandwidths of 0.02 and 1 MHz respectively and both are too narrow, not suitable for the LTE system. Literature[7] demonstrates a 3 MHz bandwidth, but at the costs of low peak SNDR of 57.8 dB and somewhat high power consumption of 11.8 mW. Literatures[9-13] also suffer from high power dissipation and bigger chip area. The evaluating FOM indicates the overall performance.

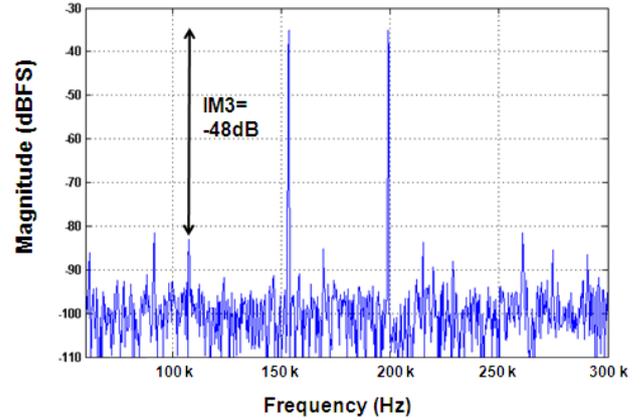


Figure 14. Two tone test (input signals:153 kHz, 199 kHz with 0.144 Vp-p)

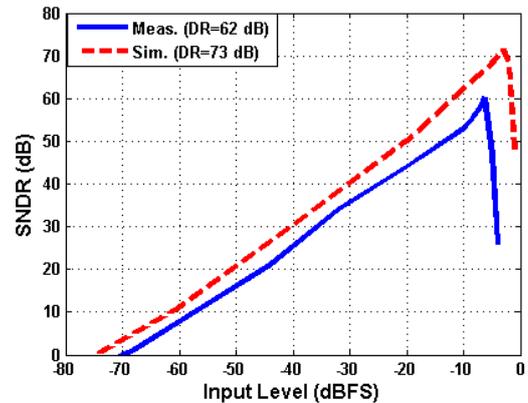


Figure 15. SNDR with varying input level

The power consumption is dominated by the amplifiers. At 1.8 V supply voltage, the measured power dissipation is less than 9 mW of which over 88% is dissipated in the op amps and their bias circuitry and about 12% is dissipated in the remaining circuits including D-latch 8.7%, ADC 3.1% and comparator 0.2%. Figure 16 illustrates the reported dissipation matched the expected value based on the simulation and analysis. Figure 17 shows a comparison to the state of the art design FOM.

Table 2. Comparison with Previously Published Papers

	This work	[7]	[8]	[9]	[10]	[11]	[12]	[13]
Process (μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Supply Voltage (V)	1.8	1.8	1.8	1.8	1.2	1.8	1.8	1.8
Clock Rate (MHz)	128	100	2.56	100	240	360	800	100
Bandwidth (MHz)	2.0	3	0.02	1	7.5	18	10	2
Peak SNDR (dB)	60.26	57.8	65.3	56.8	67	62.5	68.4	67.7
ENOB (bit)	9.72	9.31	10.55	9.14	10.84	10.1	11.07	10.9
DR (dB)	62	58	71	60	77	68	70	-
Power (mW)	9	11.8	0.42	22.2	89	183	160	68
Chip Area (mm^2)	0.64	1.67	0.21	1.62	1.4	0.68	2.5	3.2
FOM (pJ/step)	2.67	3.1	3.63	19.6	3.24	4.63	3.72	8.9

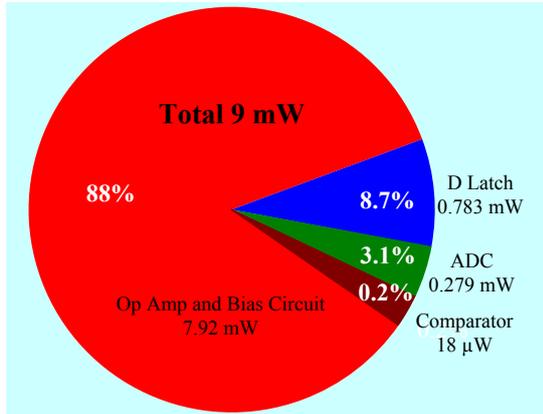


Figure 16. Pie chart distribution of area and power consumption

The FOM of (5) is given over the achieved bandwidth of recently reported $\Sigma\Delta$ modulators. This work achieves the lowest power consumption of 9 mW and the best FOM of 2.67 pJ/conv while attaining highly comparable performances in signal bandwidth, peak SNDR and ENOB.

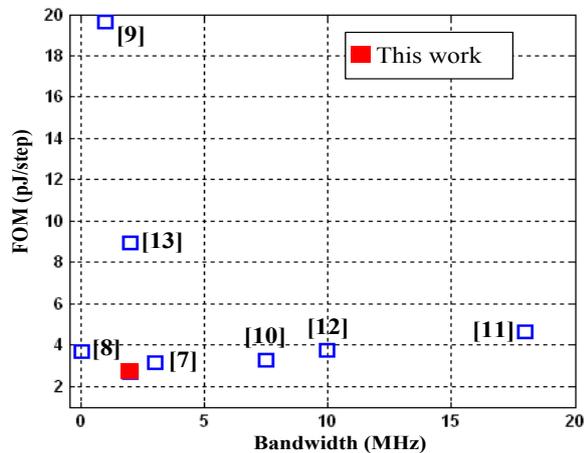


Figure 17. Comparison to the state of the art design FOM.

5. Conclusions

A low power CT $\Sigma\Delta$ modulator with a hybrid loop filter is implemented in a TSMC 0.18 μm technology. To erase the summation amplifier, the capacitive feedforward structure is employed. To reduce layout area, local feedback resistors are designed to form an active bridge-T network. The proposed hybrid CT $\Sigma\Delta$ modulator establishes better performance compared with other active counterparts. Measured results achieve the best FOM of 2.67 pJ/conv, an ENOB of 9.72-bit and a SNDR of 60.26 dB over a signal bandwidth of 2 MHz while consuming 9 mW from a 1.8 V supply voltage. The overall chip area is only 0.642 mm^2 . Compared with active $\Sigma\Delta$ modulators, the proposed $\Sigma\Delta$ modulator features less hardware complexity because the hybrid loop filter includes two passive filters, which are very simple to implement.

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