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Reliability and Retention of Floating Body RAM on Bulk FinFET

M. Aoulaiche[1,*], E. Simoen[1], Ch. Caillat[2], N. Collaert[1], G. Groeseneken[1], M. Jurczak[1]

[1]Imec, Kapeldreef, 75, 3001 Leuven, Belgium
[2]Micron Technology Belgium, Kapeldreef 75, 3001 Leuven, Belgium
Marc.Aoulaiche@imec.be

Abstract This paper assesses one Transistor Floating Body Random Access Memory (1T-FBRAM) in Bulk FinFET devices as a candidate for conventional DRAM replacement in the future technology nodes. For the cell operation, Bipolar Junction Transistor (BJT) programming is used. Reliability and retention time of the floating body effect are studied on different gate lengths, fin widths and for different programming biases. The degradation mechanisms during cycling are identified. The optimum number of cycles extracted (~10^9) is still far below the 10^{16} cycles expected. Long retention times are obtained; however, with the tail bit distribution below the 64ms DRAM specifications. Besides, the generated floating body takes place beneath the drain at the n+/p+ drain/ground-plane junction, which explains the long retention times by the large junctions area. Moreover, the floating body can be obtained only by leaving floating the bulk contact of the bulk FinFET cell, which makes its integration in a DRAM chip challenging. On the other hand, the bulk FinFET device shows a biristor like behaviour but featuring more options by the use of the gate to control the write and read.

Keywords Bulk Finfet, BJT, Cycling, Endurance, Floating Body, RAM, Retention

1. Introduction

One transistor capacitor-less random access memory (1T-RAM) is considered as a candidate to replace the conventional one transistor and one capacitor 1T/1C DRAM, which suffers from the scaling challenges related to the capacitor integration[1,5]. Various device architectures are considered: bulk, Silicon On Insulators (SOI), double gate, surround-gate etc[6-9]. Among these different architectures bulk FinFET is particularly attractive since it is going to be applied to a mass production, is more scalable than planar bulk devices, can be cointegrated with planar bulk devices and avoids the heat dissipation problem, which is present in SOI FinFET devices. Besides, different biasing schemes are proposed. With regard to the state-1 programming method: impact ionization and band-to-band tunnelling are the main mechanisms to create excess holes in the floating body[10]. On the other hand, with regard to the read method, two groups can be noticed: in the first group (Gen1), the floating body charge induces a threshold voltage shift, which changes the MOSFET current. The second group (Gen2), which is proven to improve 1T-DRAM performances and provide fast read and better scalability[4,7] uses the Bipolar Junction Transistor (BJT) present in the MOS structure.

* Corresponding author:
marc.aoulaiche@imec.be (M. Aoulaiche)
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To be viable, 1T-DRAM candidate has to satisfy conditions such as: high scalability, low intrinsic variations, high programming speed, high sense margin, long retention time and good endurance.

This paper investigates the retention and reliability of 1T-FBRAM on bulk FinFET devices. In section 2, the device fabrication and the experimental conditions are described. In section 3, the operating conditions and biases are depicted. In section 4 and 5 endurance and retention are respectively discussed.

2. Device Fabrication and Experimental Conditions

The devices are fabricated on bulk Si-substrate with doped ground plane, as illustrated in Fig.1. Fin widths down to 10nm for a fin height of H_{FIN}=60nm were made using 193nm lithography. The gate electrode consists of a 5nm SiO_2 capped with 5nm PE-ALD TiN and 100nm poly. After gate patterning, the extensions were implanted and the nitride spacers were formed. No selective epitaxial growth (SEG) was done on the source/drain areas. A NiPt-based salicide process was used after the deep S/D implants which were activated by a spike anneal. Finally, a standard Cu back-end-of-line process was used to finish the devices[6].

The measurements of the Floating Body Random Access Memory (FBRAM) were performed by applying short pulses at the drain and gate terminals, while keeping the bulk con-

tact floating. The source current is measured during the read pulse using a current amplifier. All the devices measured consist of five fins, as shown in Fig.2.

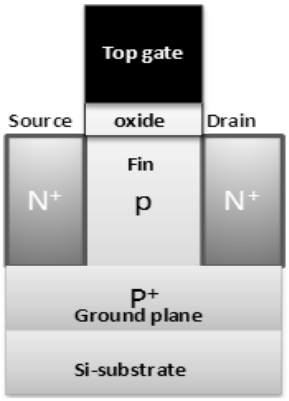

Figure 1. Lateral view of one fin cut along the channel from the source to drain

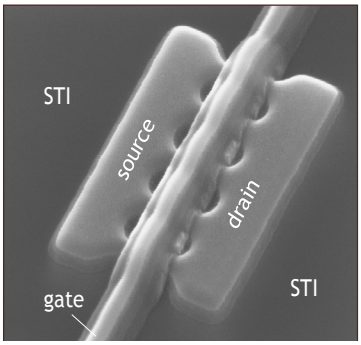

Figure 2. SEM view of a typical 5 fin bulk FinFET investigated

Endurance measurements are performed by applying a repetitive cycle to the transistor and recurrently, after a certain number of cycles, the read current for the state-0 and state-1 is measured. In this study, one cycle corresponds to a sequence write-1/read-1 and write-0/read-0, where read-0 and read-1 are the BJT currents measured for the state-0 and state-1, respectively. The cycling failure is extracted when either the state-0 or 1 shifts by 50% ΔI_S, with ΔI_S is the measured current difference between the state-0 and 1 before cycling.

The retention time is measured by increasing the holding time between a write and a subsequent read. Similarly to the cycling, the retention time is extracted at 50% ΔI_S.

3. Operating Conditions

A double sweep of the I_D-V_{GS} characteristic of bulk FinFET devices with the substrate contact grounded or left floating and at high V_{DS} exhibits a large hysteresis, as shown in Fig.3. Moreover, a high current difference between the low and high state is measured. Therefore, this bistable effect is used for the floating body memory programming. During forward sweep, when the gate bias is close to the transistor threshold voltage (V_{tf}), holes are generated by impact ionization near the drain. These holes are injected into the substrate and raise the body potential, and then the parasitic BJT is turned on. During the V_G sweep-back the holes injected by impact ionization keep the BJT current on (state-1) until the positive feedback loop between the impact ionization current and the source-bulk junction forward bias cannot be sustained anymore. Hence, below V_G= V_{tb} the BJT current turns off (state-0)[11].

The operating biases used in the dynamic operation and reproducing the floating body effect observed in DC operation are shown in Fig.4.

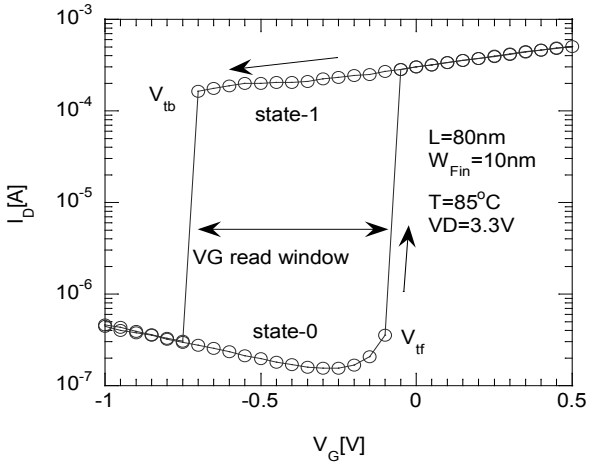

Figure 3. Double sweep I_D-V_{GS} measured on a bulk FinFET with L=80nm, W_{Fin}=10nm and at T=85℃, showing the BJT current off (state-0) and on (state-1)

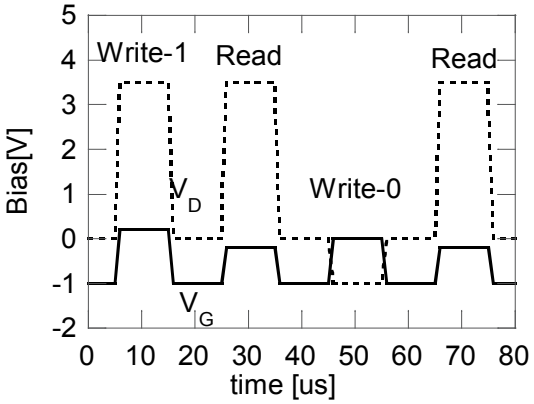

Figure 4. Schematic of the operating biases applied to the cell during write, read and cycling. The substrate is left floating.

To read, V_D is set high to trigger the parasitic BJT and V_G is defined within the hysteresis window (V_{tf}-V_{tb}). The read drain current follows the expression[12],

$$I_{D,read} = M(I_{ch} + I_{BJT}) = \frac{M}{1-\beta(M-1)} I_{ch} \quad (1)$$

where M is the impact ionization factor, β is the current gain of the BJT, I_{ch} is the channel current and I_{BJT} is the BJT current.

To write a state-1 (write-1), holes are generated by impact ionization using a high V_D and V_G higher than V_{tf}, satisfying the condition for turning on the BJT,

$$\beta(M-1) \sim 1 \quad (2)$$

To write state-0 (write-0), the holes are removed by forward biasing the drain-substrate junction.

The bulk FinFET DC hysteresis related to the parasitic BJT is measured versus gate length and fin width to find the operating biases. The results are shown in Figs.5 and 6.

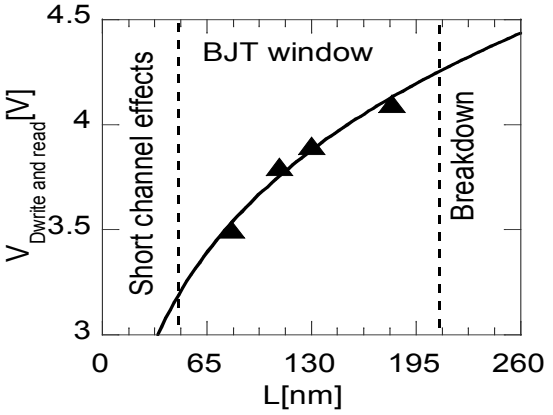

Figure 5. Gate length dependence, of the V_D bias used for the write and read with BJT programming

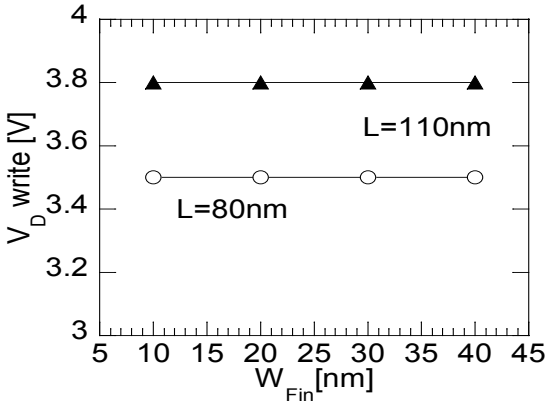

Figure 6. V_D write bias as a function of the fin width and for fixed L=110nm and 80nm

Fig.5 shows the V_D applied during write-1 or read as a function of the gate length. V_D is decreased as L is decreased. This is consistent with larger β and M in shorter gate lengths[11]. The decrease of the V_D write bias with the gate length follows the same trend as the common-emitter break down voltage with open base (BV_{CEO}), as shown in Fig.5 by the continuous line[13]. On the other hand, the BJT operation is limited by the short channel effect and by the break down for longer L[13]. For very short channels, the source-drain punch-through occurs and the channel cannot be controlled. In this case, the current always flows between the source and drain, even at low V_D. For long channel devices over 130nm, to reach the maximum lateral field needed to induce the impact ionization, a high V_D is required (> 4V) as seen in Fig.5. Therefore, the high transverse field between the drain and gate causes the device breakdown. In the case of the fin width, it has been reported that floating body effect is reduced in devices with narrow channels due to the dopant out diffusion, resulting in a carrier lifetime reduction along the channel edges[14]. In the device investigated here and for the fin widths considered, no impact of the fin width is observed. The V_D at which the BJT current is triggered, is constant for the different fin widths, as shown in Fig.6.

4. Endurance

Since the write-1 and read mechanisms use impact ionization, which is known as a reliability issue[15], endurance and the impact of the gate length and fin widths using the biasing conditions shown in Figs. 5 and 6 are investigated.

Degradation mechanisms

Fig.7 and 8 show the I_D-V_{GS} characteristics shifts under a constant voltage stress at (V_G=0V, V_D=-2V) and at (V_G=0V, V_D=3.2V) corresponding to the write-0 and write-1 condition, respectively. No significant impact of the stress under the write-0 is observed as a function of the stress time (see Fig.7). However, a small shift towards more positive V_G is observed, indicating a negative charge generated by the stress. Conversely, a large shift in I_D-V_{GS} characteristics to more negative V_G is observed under the stress in the write-1 condition (see Fig.8). This confirms that the dominant degradation is generated during the write-1 condition, where impact ionization is used.

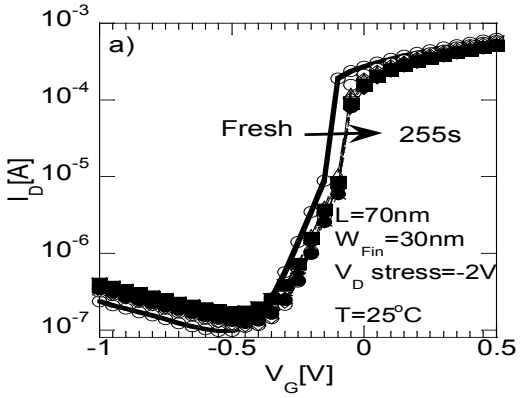

Figure 7. I_D-V_G characteristics measured at different stress times under the write-0 stress condition (V_G=0V, V_D=-2V)

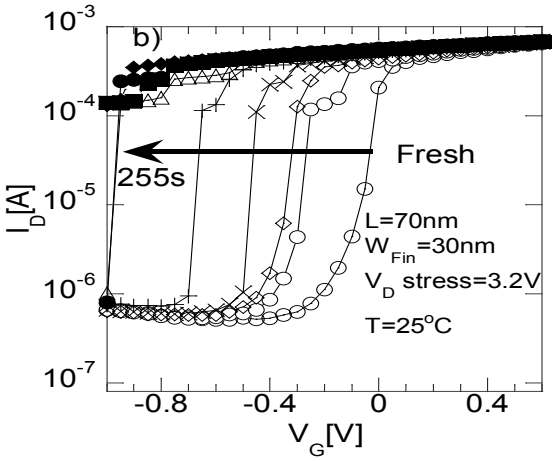

Figure 8. I_D-V_G characteristics measured at different stress times under the write-1 stress condition (V_G=0V, V_D=3.2V)

The shift of the I_D-V_G characteristics to more negative V_G indicates positive charge generation. Most probably, this is related to hot-hole-induced damage[16]. Indeed, an increase in the current of holes tunnelling to the gate can be observed during the hysteresis measurements, as shown in Fig.9.

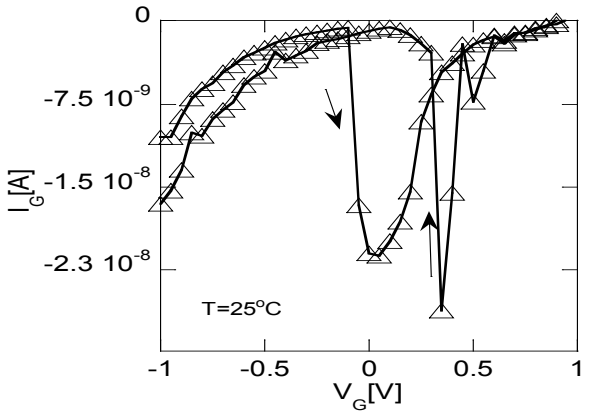

Figure 9. Gate current measured as a function of V_G during the hysteresis measurement as shown in Fig.3, showing hole tunnelling to the gate

To evaluate the Si/SiO_2 interface degradation, the charge pumping (CP) current is measured before and after stress in the write-1 condition. Furthermore, after the stress, the CP measurement is performed with source or drain disconnected in order to identify where the defects are generated, either close to the drain or source[17]. Interface states generation is observed as shown by the increase of the charge pumping current in Fig.10. Moreover, when the drain contact is disconnected during the measurement after the stress all the defects close to the drain did not contribute to the measured current (Fig.10). However, when the source contact is disconnected no difference is observed. Accordingly, the interface defects are generated close to the drain, which is consistent with impact ionization occurring in the depletion region close to the drain[18].

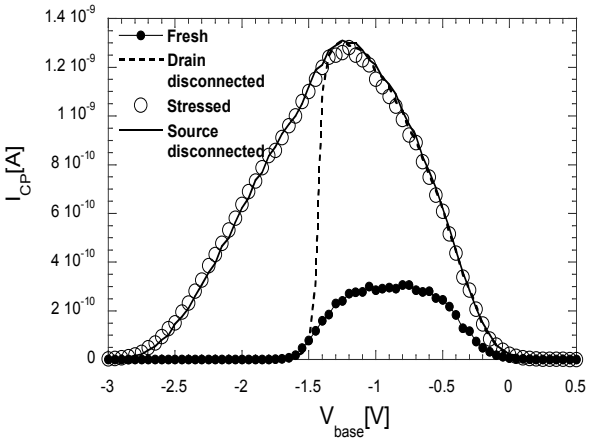

Figure 10. Base level sweep charge pumping current measured before and after stress under high drain bias of a device with 65nm height, W_{Fin}=0.25μm and L= 1μm at 25℃

Furthermore, the normalized charge pumping current before and after stress showed a slight shift in the CP curve to more negative base level voltage, which is likely related to positively charged oxide traps, either filled or generated by hot holes injection, which is consistent with holes tunnelling to the gate as shown in Fig.9. Consequently, during the write-1 condition at high drain bias and low gate bias, hot hole injection is occurring and causing interface defects generation close to the drain. Moreover, for a high transverse electric field between the drain and the gate, hot holes are injected into the dielectric and probably generate or fill positively charged oxide traps.

Cycling dependence on the gate length and fin width

Fig.11 shows the cycling failure behaviour as a function of the gate length, for a fixed fin width of 20nm. Three different regimes are observed as a function of L. In the first regime, the number of cycles to failure increases with L till an optimum, here L=130nm for W_{Fin} of 20nm. In the second regime, the number of cycles decreases. In the third regime, the device breaks after a few cycles.

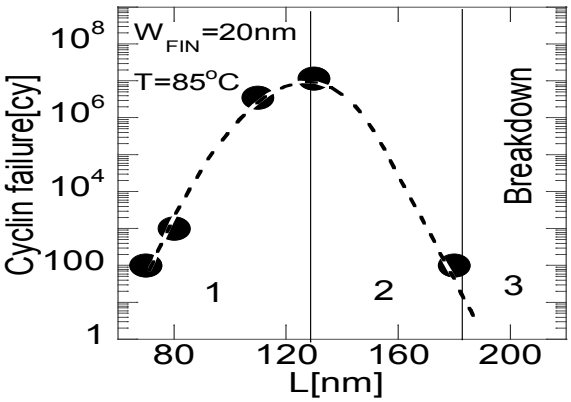

Figure 11. Cycling failure extracted at 50% ΔI_S shift and for different gate lengths. 1 cycle corresponds to the scheme in Fig.4

Different cycling failures are observed for the different regimes shown in Fig.11. Fig.12 shows the cycling failure observed for shorter channel devices, typically below L=90nm. The cycling failure is caused by the state-0 degradation. For the reason that the generated defects are located close to the drain, they further increase the drain-induced barrier lowering (DIBL) in the short channel devices, which results in a much larger threshold voltage (V_{th}) decrease. As the read is done at a fixed negative V_G, the subthreshold current measured during read-0 increases and induces the cycling failure. Fig.13 shows the cycling failure kinetics for devices with L higher than 90nm and below 130nm. The cycling failure is due to the state-1 degradation. In this case, the positively charged defects close to the drain have less impact on the lateral field. However, by increasing the number of cycles, the BJT current gain β is degraded due to hot holes[19, 20]. The decrease of the number of cycles in the second regime for increasing L can be explained by the high transverse electric field between the drain and the gate. For increased V_D bias (see Fig.5), holes generated by impact ionization close to the drain gain more energy to cross the SiO_2 potential barrier and generate

oxide defects. Consequently, the cycling number is reduced with the increase of L. The change of the cycling behaviour, which is seen in Fig.13 for L=130nm or longer, indicates that hot hole tunnelling from the drain to the gate is dominant. For L higher than ~ 180nm both states 0 and 1 fail, as shown in Fig.14. This is due to the device breakdown.

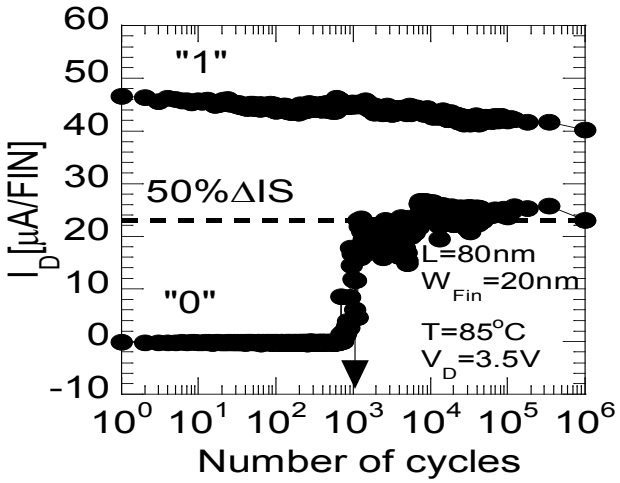

Figure 12. State-1 and 0 shifts as a function of the number of cycles, showing the state-0 degradation

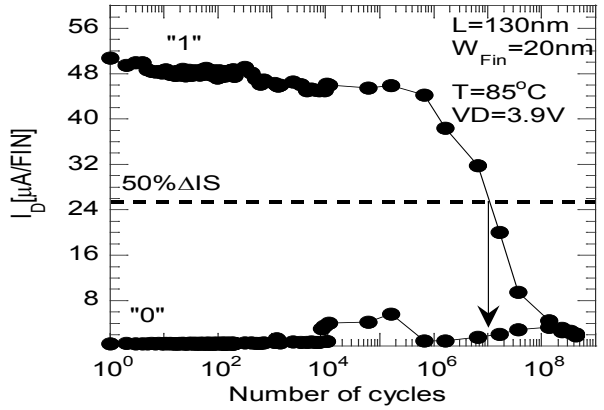

Figure 13. State-1 and 0 shifts as a function of the number of cycles, showing the state-1 degradation

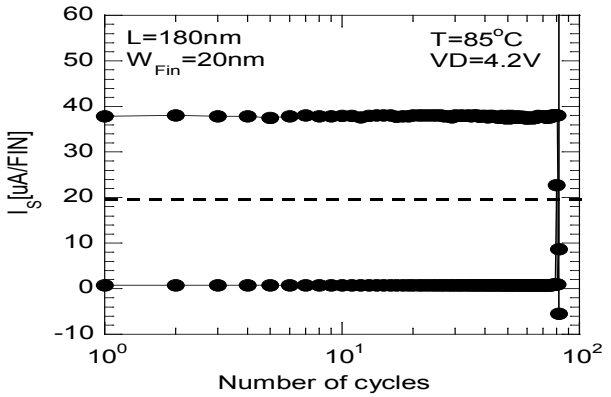

Figure 14. State-1 and 0 measured as a function of the number of cycles, showing the state-0 and 1 failure

Fig.15 shows the cycling failure measured at 85°C for L fixed at 110nm and W_{Fin}=20, 30 and 40nm and for an L=90nm and W_{Fin}=90nm. The number of cycles to failure is increased with the increase of W_{Fin}. However, a saturation trend is expected from Fig.15. The possible reasons for the increased degradation in narrower fins are the corner effect, the stress induced by the shallow trench isolation and a higher degradation in the side walls, which have different surface orientation compared to the top interface[21].

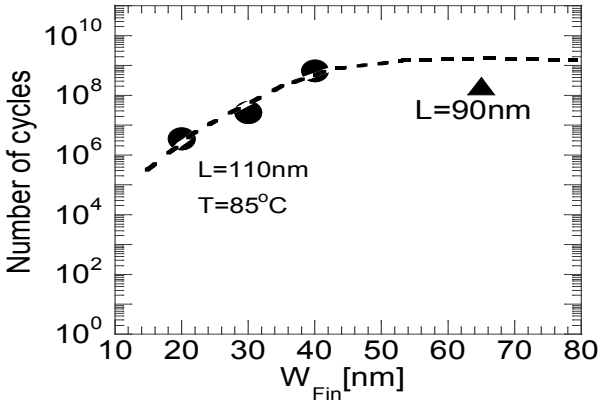

Figure 15. Cycling failure extracted a 50% ΔI_S shift as a function of the fin width

5. Retention

The retention distribution of 30 devices measured over the wafer is shown in Fig.16. High retention times are observed. However, the distribution is over ~5 decades of time, from 0.2ms to 10s.

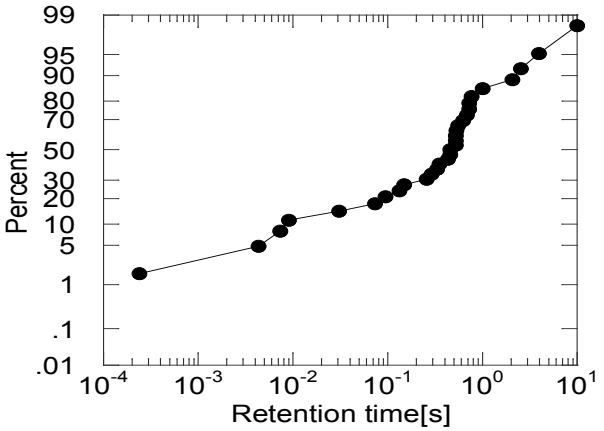

Figure 16. Retention time distribution measured on 5 fin bulk FinFET devices with L=80nm and W_{Fin}=30nm at 85℃

Retention dependence on the gate length and fin width

The retention time as a function of the gate length is shown in Fig.17 and as a function of the fin width in Fig.18. Due to the large retention time distribution shown in Fig.16, it is hard to conclude about the L and W_{Fin} impact on the retention time. However, it is observed that the retention time is lower for the shorter gate length, which is consistent

with the short channel effects and the increase of the junction leakage. On the other hand, no trend is observed versus W_{Fin} for the retention time whereas the impact on the sense margin is significant. This could be correlated to the reduced impact ionization with the reduced fin width[22].

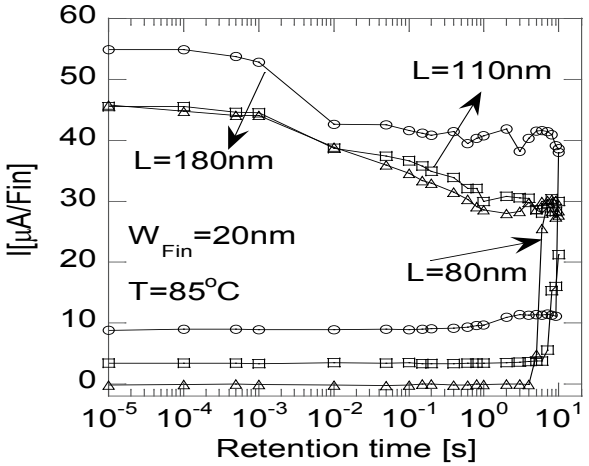

Figure 17. Retention time measured on bulk FinFET devices with fixed W_{Fin}=20nm and different gate lengths at 85℃

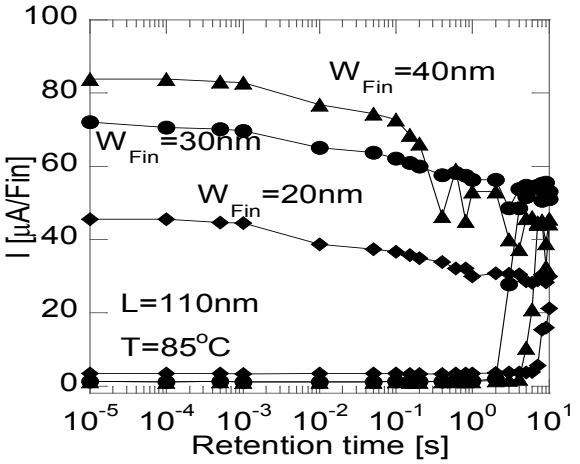

Figure 18. Retention time measured on bulk FinFET devices with fixed L=110nm and different fin Widths at 85℃

Retention dependence on the operating biases

Contrary to the DC hysteresis shown in Fig.3 which can be measured with the substrate grounded or left floating, for the dynamic operation, if the bulk contact is grounded, then the floating body effect vanishes, as shown in Fig.19. For dynamic measurements, between the write and read the device is held at negative V_G and source, drain and bulk are grounded. During this holding time, the injected holes leak to the substrate contact. In DC measurements V_D is kept constant during V_{GS} sweep forth and back, therefore the BJT feedback loop remains active and is observed even when the bulk contact is grounded. Fig.20 shows the DC hysteresis measured with the substrate contact grounded. The generated holes are injected into the gate, into the substrate and into the channel, i.e., a hysteresis loop is measured in the four device terminals. Electrons are flowing to the drain and holes are injected to the bulk to the gate and to the channel. Till the triggering point, the hole current flowing to the bulk is dominant and beyond, holes flowing to the source take over (channel).

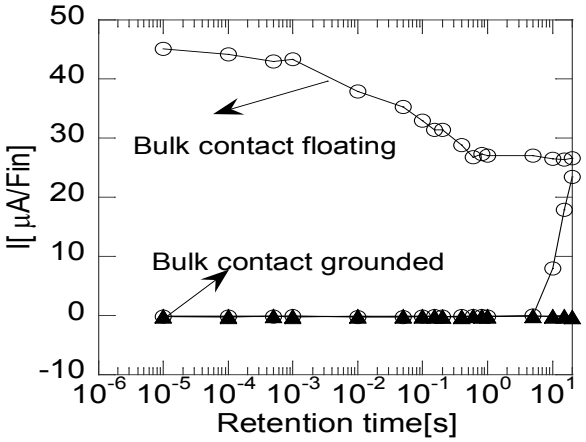

Figure 19. Floating body retention time measured with the bulk contact floating and grounded on a bulk FinFET device with W_{Fin}=20nm, L =80nm and at 85℃

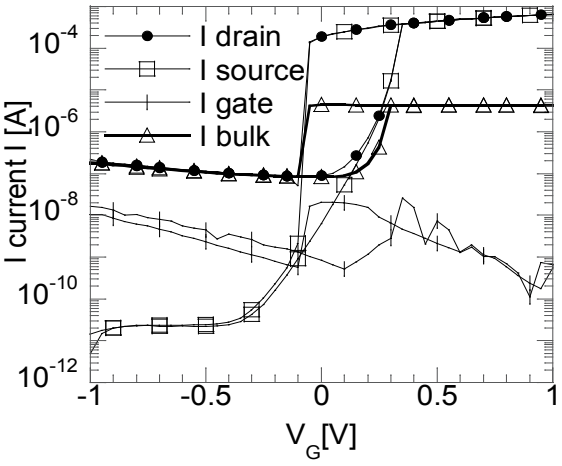

Figure 20. DC hysteresis measured on a bulk FinFET device with W_{Fin}=20nm, L=110nm, at V_D=3.5V and at T=25℃

On the other hand, using pulsed measurements (see Fig.4) and with the bulk contact floating, no effect of the V_G holding bias is observed, for V_G hold varying from -2V to 2V, as shown in Fig.21. This indicates that the holes resulting in the floating body are not stored in the FinFET channel (in the fin) but most probably between the drain and ground plane, n^+-p^+ junction (See Fig.1). Indeed, storing holes in the fin requires being in accumulation or having a partially depleted film, but 20nm-wide FINs with their gate biased to +2V do not fulfil this requirement: they are in Full Depletion. As it has been previously reported[23], in such a case, the holes can be stored only below the FIN itself, in a P-type region. In our case, the P+ ground plane has to be floating to avoid hole recombination, since it is not isolated from the Si–Substrate (see Fig.1). Moreover, this is consistent with the fact that the operating bias V_D and the retention time are independent of

the fin width. Furthermore, the long retention times measured (~10s) are probably due to the large junction area in the FinFET with 5 fins, much greater than the MOS capacitance of the fins.

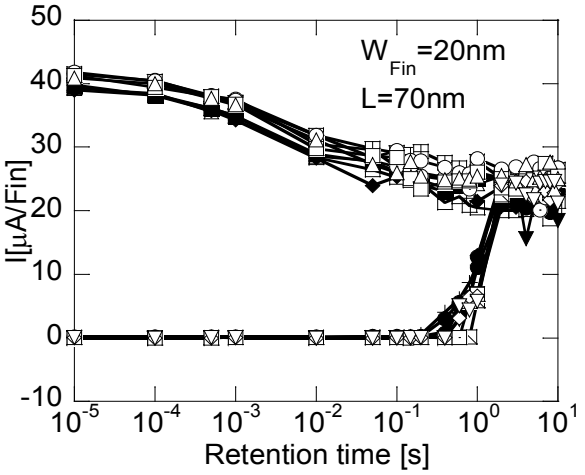

Figure 21. Retention time measured for V_G hold varying from -2V to +2V, showing no effect on the stored holes

Finally, Fig.22 shows that the Bulk FinFET device behaves as a biristor[24]. Even with both gate and bulk left floating, a floating body and retention time are measured. However, compared to the biristor the write and read can be controlled by the gate, which can be a useful feature.

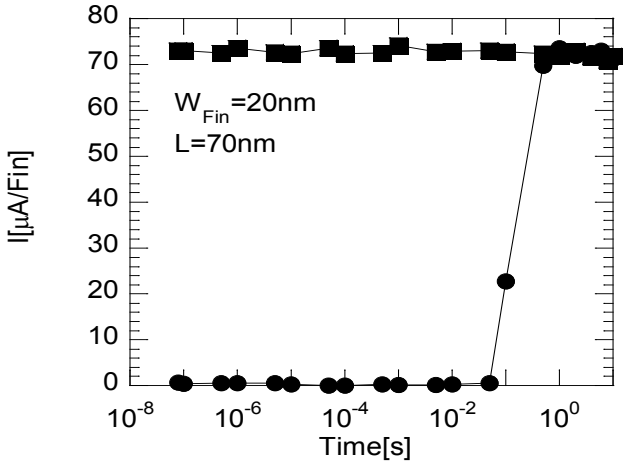

Figure 22. Retention time measured on a bulk FinFET with the gate and bulk contact left floating

6. Conclusions

The floating body effect in bulk FinFET devices is investigated for 1T-DRAM application, using the BJT programming mode. High memory window and sense margin are observed as expected from the BJT programming. However, during cycling the sense margin is degraded due to interface defects generation and positively charged traps close to the drain, where hot holes are generated during the write condition of the state-1. The cycling failure is observed depending on the fin length and width. Nevertheless, the optimum number of cycles (~10^9) remains below the 10^{16} expected by conventional DRAM specifications. Besides, long retention times (~10s) can be obtained. However, the tail bit distribution is below the 64ms DRAM requirement. It is also shown that the floating body effect is due to holes stored in the ground-plane below the drain junction and not in the fin volume of the bulk FinFET. Therefore, the floating body effect disappears for grounded bulk FinFET cells what enhances the challenge of 1T-FBRAM chip fabrication. Furthermore, similar behavior of the floating body as in a biristor is observed when leaving the gate and bulk contacts of the bulk FinFET device floating.

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