

Gate Leakage Current in GaN HEMT's: A Degradation Modeling Approach

A. Mimouni^{1,*}, T. Fernández¹, J. Rodriguez-Tellez¹, A. Tazon¹, H. Baudrand², M. Boussuis³

¹Departamento de Ingeniería de Comunicaciones-Universidad de Cantabria Laboratorios I+D+i de Telecomunicaciones, Santander, 39005, Spain

²Henri Baudrand Laboratoire LAPLACE-GRE ENSEEIHT 2, BP 7122, 31071 Toulouse CEDEX 7, France

³Département de Physique, Université Abdelmalek Essaâdi, Faculté des sciences Tétouan, 93030, Maroc

Abstract In this paper we present an empirical preliminary model able to simulate the degradation with time in the gate leakage current in GaN HEMT devices. The model is based on extensive reverse and forward current measurements, carried out on a wide range of different device designs and under different bias, performed over aged transistors by III-V Lab (Alcatel-Thales) within the European KORRIGAN. A closed form expression for the reverse gate current, depending on time, as well as the expression parameters extraction procedure are presented. The experimental and simulated results presented illustrate the validity of the model as well as it's usefulness in reliability studies.

Keywords Leakage Current, GaN HEMT, Modeling

1. Introduction

In applications such as high-power and high-frequency amplifiers for base stations AlGaIn/GaN HEMT devices offer the circuit designer certain advantages over the more traditional GaAs devices. These mostly relate to the ability of these devices to handle high operating voltages under high current conditions. Their main drawback, however, relates to their reliability which needs to improve considerably[1]. While reliability issues have been considered by others on AlGaIn/GaN devices[2-5] the emphasis of the work has been on the degradation in the output current, the power dissipated and the drain resistance R_d of such devices[6]. The degradation effects on the gate leakage current arises as an important feature when studying GaN HEMT reliability[7-12], being worthy of note its effect on the saturation current and breakdown voltage parameters of the device[13].

In this paper we present an empirical model able to simulate the degradation in the gate leakage current with time on AlGaIn/GaN devices. The model presented in this work is based on extensive experimental measurements carried out by III-V Lab (Alcatel-Thales) within the European KORRIGAN project on many specimens over prolonged periods of time (2000 hours).

2. Gate Leakage Current

As stated previously, AlGaIn/GaN HEMT devices are well suited to high-power high-frequency applications such as high power amplifiers and applications for wireless base stations. For such cases there is a general requirement for a low input gate current and a high reliability figure for the device. In previously reported work[14] the role played by the degradation with time in the gate leakage current is important in the understanding of the reliability issue for the device.

From a physical point of view the degradation, and hence changes observed with the device, arise from defects under the gate region. These become more evident at a critical point in the value of the electric field[13-14]. Trap formation in the device at either the semiconductor surface or within the bulk is also a performance-limiting issue. To date, however, a clear explanation for the physical mechanisms which ties together the failure or reliability of the device and the degradation in it's electrical characteristics is unavailable.

The gate leakage current surges as a consequence of surface processing and passivation issues. In Field Effect devices quantum mechanical tunnelling has been clearly shown to be an important effect to be accounted for[13]. For example, electrons tunnelling from the gate can create a gate-to-drain leakage current by hopping from trap to trap. Alternatively, the electrons can accumulate on the surface next to the gate or move through the AlGaIn layer to the conducting channel[15].

* Corresponding author:

ami27@alumnos.unican.es (A. Mimouni)

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A model to simulate the gate leakage current in GaAs MESFET's due to tunnelling effects is described in [16]. This model was subsequently altered in [17] to be applicable to GaN devices.

The gate leakage current due to tunnelling effects is represented in circuit form as a generator connected between the gate and drain terminals of the device. The electric field at the edge of the gate terminal is reduced by the electrostatic feedback. This reduces the electron tunnel leakage current. As the number of electrons increases at the gate edge as a function of time the gate leakage current reduces due to the feedback. In addition, the increased electron density on the AlGaIn surface decreases the number of 2DEG electrons and this causes the gate current to decrease [15-16].

3. Gate Leakage Current Degradation Model

The leakage mechanism in GaN and AlGaIn Schottky interfaces was considered by Yu et al [18] and Miller et al [19]. This work was based on field-emission tunnelling transport assuming a triangular Schottky potential distribution. To obtain good agreement with experimental results, however, requires a value for the donor density which is higher than in practice. This led them to suggest a defect-assisted tunnelling mechanism to increase the leakage current.

A surface patch model was proposed by Sawada et al [20] to explain the forward current characteristics. Miller et al [21] have also proposed a leakage mechanism associated with a variable-range hopping conduction through threading dislocations.

As will be demonstrated later, we have found the thermionic field emission (TFE) model to provide a good compromise between accuracy and ease of parameter extraction.

In the TFE model, the reverse current, $I_{g leak}$, arises from electrons that are thermally excited from the metal Fermi junction and tunnel through the semiconductor depletion layer to the semiconductor conduction band [22].

The reverse current can be expressed by the following equations [22]:

$$I_{g leak} = I_{s, TEF, r} \exp\left(\frac{V_r}{\varepsilon'}\right) \quad (1)$$

Where:

$$I_{s, TEF, r} = \frac{AA^* T^2 \sqrt{\pi E_{00}}}{V_t \cosh(E_{00}/V_t)} \exp\left(\frac{\phi_{Bn}}{E_0}\right) \sqrt{\phi_{Bn} - V \cosh^2(E_{00}/V_t)} \quad (2)$$

$$E_0 = \frac{E_{00}}{\tanh(E_{00}/V_t)}$$

$$E_{00} = \frac{qh}{4\pi} \sqrt{\frac{N_d}{m^* \varepsilon_s}}$$

$$\varepsilon' = \frac{E_{00}}{E_{00}/V_t - \tanh(E_{00}/V_t)}$$

Where V_r is the reverse bias, A is the area of the diode, A^* is the Richardson constant, T is the Temperature of the channel, (q is the electron charge and K is the Boltzmann constant) and ϕ_{Bn} is the Schottky barrier height.

The term E_{00} is the characteristic energy related to the tunneling probability in the Wentzel-Kramers-Brillouin approximation which depends on the donor density N_d .

From the life tests (electrical and thermal aging for a total duration in the region of 2000 hours) experimental results, we observe that the most time dependent parameters were the Schottky barrier height ϕ_{Bn} and the donor density N_d [18-19].

From reverse and forward current measurements (carried out on a wide range of different device designs and under different bias) performed over aged devices, we have observed that the time dependency of parameters N_d and ϕ_{Bn} can be expressed, from a macroscopic point of view, as:

$$N_d = N_{d0} \exp\left(-\frac{t - t_0}{N_{d1}}\right) \quad (3)$$

$$\phi_{Bn} = \phi_{B0} + p_1 (t - t_0)^{p_2} + p_3 \tanh\left(\frac{t - t_0}{p_4}\right) \quad (4)$$

Where N_{d0} is the donor density at $t = 0$ h, ϕ_{B0} is the Schottky barrier height at $t = 0$ h, N_{d1} , p_1 , p_2 , p_3 , and p_4 are the parameters of the equation describing the behavior of the expression.

These expressions demonstrate that high operating temperature conditions causes important changes to the schottky barrier height and to the donor distribution. This has also been observed through the various life-tests experiments carried out on many different specimens.

4. Results and Discussion

4.1. Device description and Performed Measurements

In order to validate the approach adopted, five aged devices (two with a gate-width of 2X75 μm and three with a gate-width of 8X75 μm provided by III-V Lab (Alcatel-Thales) are employed. For these devices, forward and reverse gate current measurements are performed at our laboratories.

The 8x75 μm devices, are fabricated using an undoped multilayer structure consisting of a GaN buffer layer (1.5 μm), followed by an AlGaIn barrier layer (22.0 nm thickness, 27% Al concentration). These GaN HEMTs are fabricated on all wafers using the same industrial quality process, including ohmic contact formation through Ti/Al/Ni/Au deposition and Schottky gate electrode formation using Mo/Au deposition.

In the case of the 2x75 μm devices, the undoped multilayer structure consisted of a GaN buffer layer (1.0 μm), followed by an AlGaIn barrier layer (27.5 nm

thickness, 30.3% Al concentration). These GaN HEMTs are fabricated on all wafers using the same industrial quality process, including ohmic contact formation through Ti/Al/Pt/Au deposition and Schottky gate electrode formation using Ni/Au deposition.

During the aging test, several DC life tests are launched in order to evaluate the effect of the temperature junction on the degradation of the transistors. The different ambient temperatures of the junction are selected at 150°C, 175°C, 250°C and 300°C. The tests duration are targeted at 1000 or 2000 hours.

The bias point used in the aging test is 25V V_{ds} and I_{ds} 420 mA/mm. The drain current is kept constant by automatic gate voltage control so that the dissipated power is constant and the temperature of the junction as well. In Table 1, summarizes the test conditions for the different devices during the aging process

Table 1. Specimen measured and the life test conditions

Device	SIZE (MICRONS)	Temperature (°C)	Bias Conditions (V_{GS} , V_{DS})	Test Duration
D1	8x75	250	(-2.3 V, 25 V)	1038 hours
D2	8x75	275	(-2.3 V, 25 V)	1038 hours
D3	2x75	150	(-3.2 V, 25V)	2000 hours
D4	2x75	175	(-3.1 V, 25 V)	2000 hours
D5	8x75	175	(-3.1 V, 25 V)	2000 hours

As an example, Figure 1 shows the variation of the gate current over different aging time intervals for the 8x75 μm device. The measurements were performed as a function of V_{gs} at a V_{ds} of 25V after thermal and electrical aging at the temperature $T = 175^\circ C$.

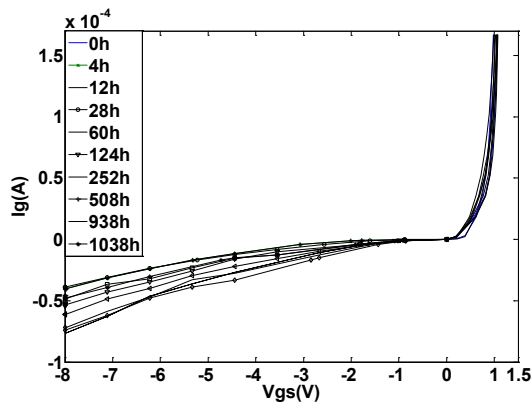


Figure 1. Measured gate current versus gate-source voltage as a function of aging time (hours) at $V_{ds}=25V$ for device D5

4.2. Extraction of the Model Parameters

Table 3. Parameters of equation 4

Device	ϕ_{B0} (eV)	P_1 (V/hour)	P_2	P_3 (V)	P_4
D1	0.86	$-5.79 \cdot 10^{-5}$	$5.567 \cdot 10^{-1}$	$1.555 \cdot 10^{-4}$	$-1.071 \cdot 10^5$
D2	0.783	$1.31 \cdot 10^{-5}$	5.50910^{-1}	$1.118 \cdot 10^{-1}$	$-1.91 \cdot 10^{-3}$
D3	0.505	$1.04 \cdot 10^{-2}$	1.19210^{-1}	-1.74510^{-2}	$1.375 \cdot 10^1$
D4	0.492	$1.20 \cdot 10^{-1}$	2.98210^{-1}	-1.28910^{-1}	$3.067 \cdot 10^{-1}$
D5	0.8819	$-1.82 \cdot 10^{-2}$	9.99110^{-2}	-3.29110^{-1}	$2.476 \cdot 10^{-5}$

In brief, the extraction of the model parameters is performed in three steps as:

(i). At time t_0 , the value of parameter ϕ_{B0} is obtained using a high precision current source. For this measurement the gate-drain junction is forward biased Figure 2 and the parameter measured under very low current conditions ($<1mA$) so that the parasitic resistance of the device has a negligible effect. Clearly this assumption is only valid under this condition and for the purpose of extracting this parameter.

(ii). The device is then aged over time according to the conditions shown in Table 1. For each device and test condition, measurements are made under forward (step (i)) and reverse bias conditions as shown in Figure 1. For each device, parameters N_{d0} (at time $t = 0$ h) and N_{d1} are determined from reverse bias measurements. Using this information parameter N_d is then calculated and optimised.

(iii). The parameters (p_1 , p_2 , p_3 and p_4) of equation (4) are obtained from forward bias measurements (Figure 2). Prior to extracting these parameters the measured current values are adjusted using the parameter values of equation (4) determined previously.

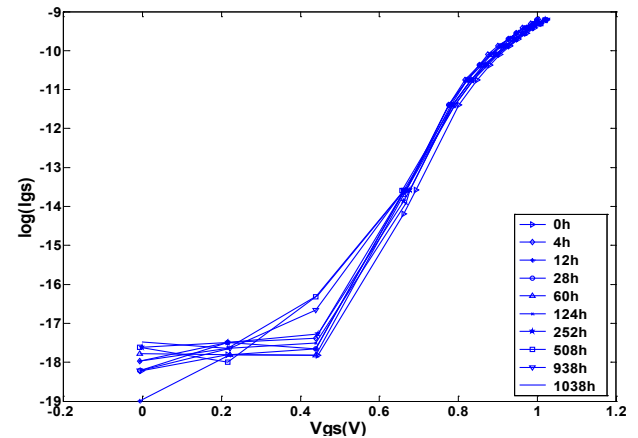


Figure 2. Forward bias measurements gate current versus gate-source voltage as a function of aging time for device D5

The results of this exercise are shown in Tables 2 and 3.

Table 2. Equation 3 parameters

Device	N_{d0} (CM ⁻³)	N_{d1}
D1	7.510^{17}	$5.559 \cdot 10^7$
D2	10^{18}	$4.559 \cdot 10^7$
D3	10^{17}	$4.113 \cdot 10^8$
D4	$9 \cdot 10^{17}$	$1.948 \cdot 10^7$
D5	$7.1 \cdot 10^{16}$	$4.559 \cdot 10^7$

Bearing in mind that the test devices considered here are N type HEMT's with Ni/Au Schottky junctions, it can be seen that the results here are in keeping with those to be expected and presented elsewhere[23]. For example, the value of ϕ_{Bn} is less than 1V. Also notice that for the 8X75 μm device the value of parameter ϕ_{B0} reduces as the ambient temperature increases. This is also in keeping with the results presented elsewhere[24, 25]. This can be explained by the fact that the additional ionized doping atoms, arising from the positive fixed charge at the surface, increases the number of ionized doping atoms at the surface. Tunnelling is, therefore, easier since the barrier is thinner at the surface.

The devices studied in this work are different transistors gallium nitride HEMT of Waffer (AEC1303) and Waffer (AEC1388) submitted to different thermal and electrical aging, as shown in the table 1; this can explain the observed differences between the value of the parameters of equation 7 for the devices studied. As an example, the value of parameter p_1 for the device D1 and D5 is negative while for the other devices is positive; and that can be explained by: the measurement results I_g with time decreases and also the first part of the equation 4 is a polynomial.

Figures 3 and 4 Show the evolution of with time for devices under test.

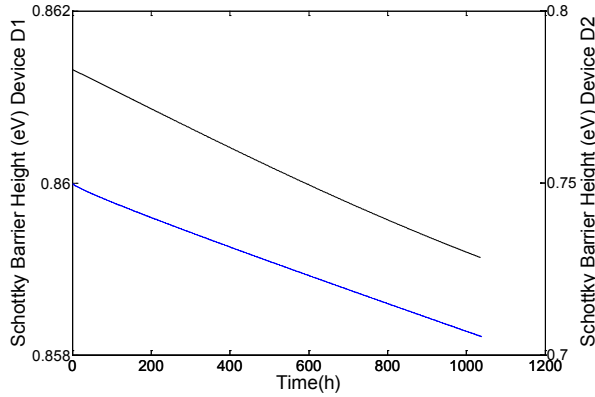


Figure 3. Time-dependent for D1 (solid) and D2 (dotted) devices

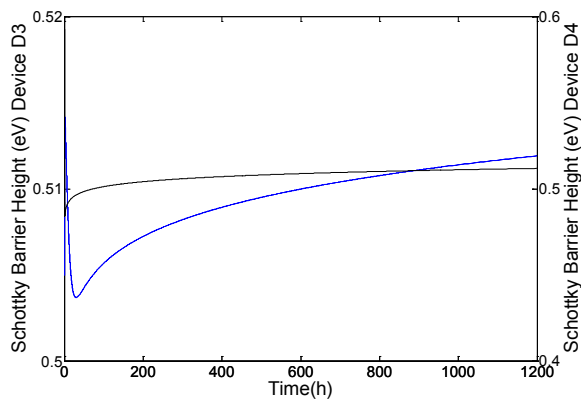


Figure 4. Time-dependent for D3 (solid) and D4 (dotted) devices

In Figures 5, 6, 7, 8 and 9 we compare the measured and computed gate leakage current using equation (1) as a

function of time for the 8X75 μm and 2X75 μm devices using the conditions shown in Table 1. The results indicate good agreement between the experimental and modelling approach. The discrepancies between the measured and simulated results are largely due to measurement errors and the optimisation strategy employed to refine the model parameter values. These two areas are under consideration taking into account the need for the model and general approach to be useful to devices fabricated by a wide range of foundry houses and processing conditions.

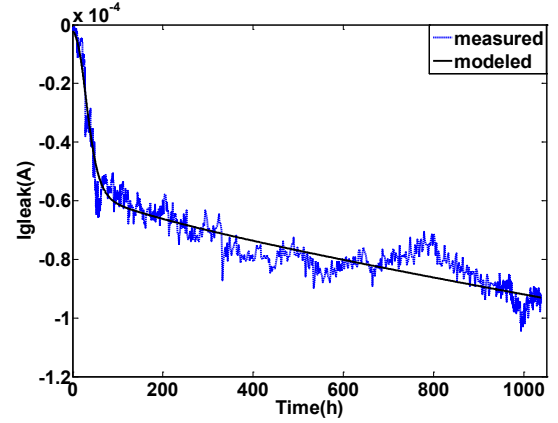


Figure 5. Modelled and measured stress time-dependent $I_{g\text{leak}}$ for D1 device

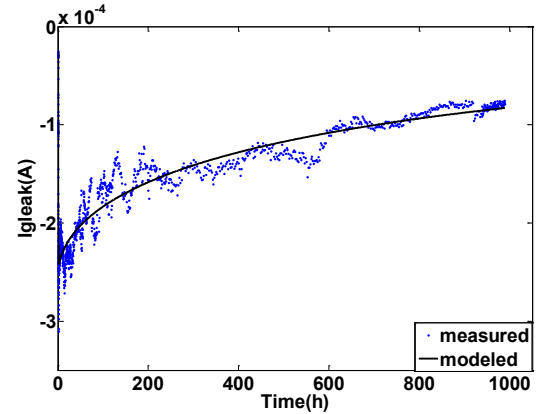


Figure 6. Modelled and measured stress time-dependent $I_{g\text{leak}}$ for D2 device

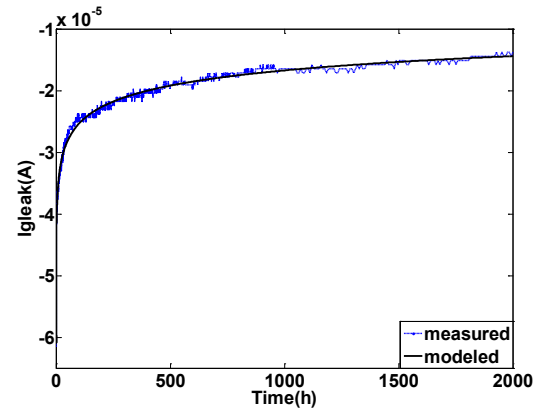


Figure 7. Modelled and measured stress time-dependent $I_{g\text{leak}}$ for D3 device

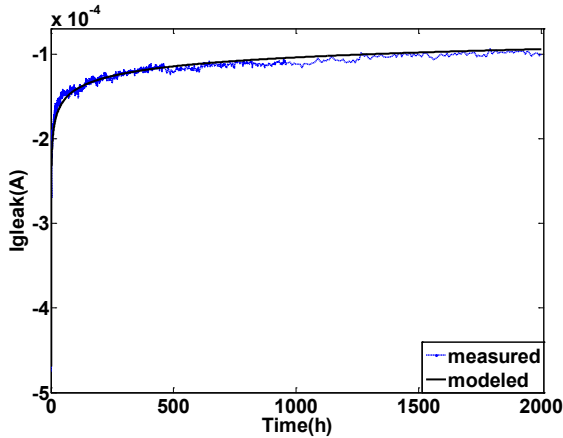


Figure 8. Modelled and measured stress time-dependent I_{gleak} for D4 device

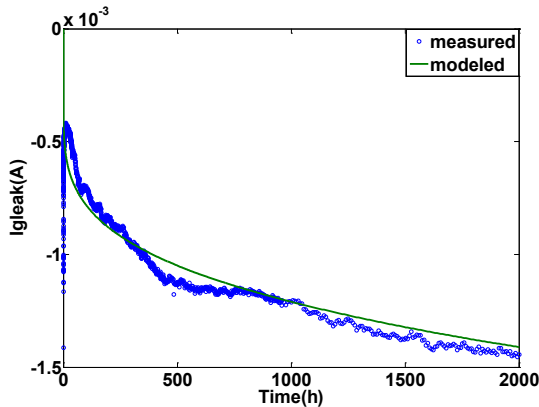


Figure 9. Modelled and measured stress time-dependent I_{gleak} for D5 device

It is interesting to observe from the results for device D4 and D5 the increase in the value of I_{gleak} and the reduction in the value of N_d as the gate area increases. It should be remembered that the measurements for these two devices are performed under identical operating conditions. These results are in keeping with those presented [26].

5. Conclusions

A model to simulate the degradation in the leakage current with time has been applied to AlGaIn/GaN HEMT devices of varying sizes from different manufacturers. These have been measured under a variety of test conditions including various ambient temperature points. The results clearly show a strong dependence between the leakage current, the barrier potential and the donor density of the gate-drain junction. These results also demonstrate the strong influence that the surface and bulk traps of the material have on the leakage current. Not unexpectedly the results also demonstrate the strong inter-dependence between these variables and the ambient temperature.

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