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Reconfigurable Voltage Mode Phase Shifter using Low Voltage Digitally Controlled CMOS CCII

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Abstract The low voltage digitally controlled current conveyors have been used to realize the digitally controlled reconfigurable continuous time first order voltage mode phase shifters. Each of the realized phase shifters uses two digitally controlled current conveyers along with three passive elements. The realized phase shifters provide digital control to phase angle through an n-bit digital control word. The realized digitally controlled continuous time phase shifters are designed and verified using PSPICE and the results thus obtained justify the theory.

Keywords Current Conveyors, Phase Shifter, Filter

1. Introduction

Introduction of digital control to the current conveyor (CCII) has boosted its functional flexibility and versatility in addition to its higher signal bandwidth, greater linearity and large signal bandwidth[1-10]. This digital control has eased the on chip control of continuous time systems through digital word with high resolution capability and reconfigurability[1-5],[10].

This paper basically deals with the realization of reconfigurable continuous time first order voltage mode phase shifters using Low voltage digitally controlled CCII. Each of the realized phase shifters uses two digitally controlled current conveyors along with three passive elements. The realized phase shifters provide digital control to phase angle through an n-bit digital control word. To verify the theory, the realized digitally controlled continuous time phase shifters are designed and verified using PSPICE and the results thus obtained justify the theory.

2. The Circuit

The digitally controlled CCII symbol is shown in "Figure 1(a)" and its CMOS implementation with 4-bit control is shown in "Figure 1(b)". The current summing network (CSN) is included at port-X[1-4],[9],[10]. The transfer matrix can be expressed as follows.

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -N & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

Thus the port voltages and currents for the digitally programmable current conveyor (DPCCII) can be expressed as $I_Y = 0$, $V_X = V_Y$ and

$$I_{Z-} = -NI_X \quad (2)$$

where, N is an n-bit digital control word.

The voltage mode phase shifters using low voltage digitally controlled CMOS DPCCII are shown in "Figure 2". The DPCCII- uses the CSN at port-Z- as shown in "Figure 1(b)". The routine analysis yields the voltage transfers function for the reconfigurable phase shifter-I of "Figure 2(a)" as

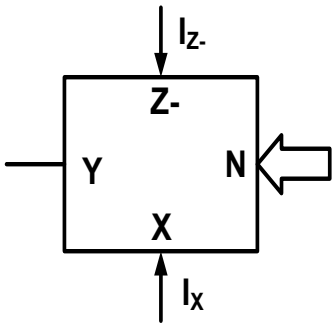

Figure 1(a). Symbol for 4-bit DPCCII-

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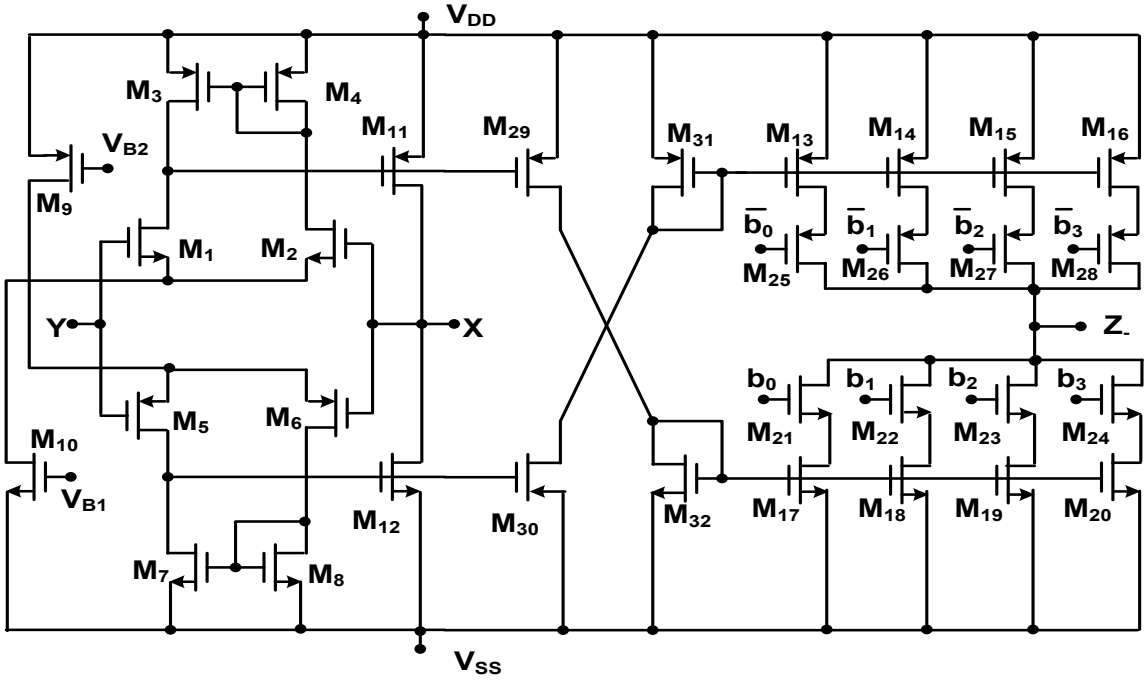

Figure 1(b). The CMOS implementation of a 4-bit DPCCII- with CSN at port Z-

The voltage mode phase shifters using low voltage digitally controlled CMOS DPCCII are shown in "Figure 2". The DPCCII- uses the CSN at port-Z- as shown in "Figure 1(b)". The routine analysis yields the voltage transfers function for the reconfigurable phase shifter-I of "Figure 2(a)" as

$$\frac{V_{OUT}}{V_{IN}} = \frac{S - \frac{N}{CR_1}}{S + \frac{N}{CR_2}} \tag{3}$$

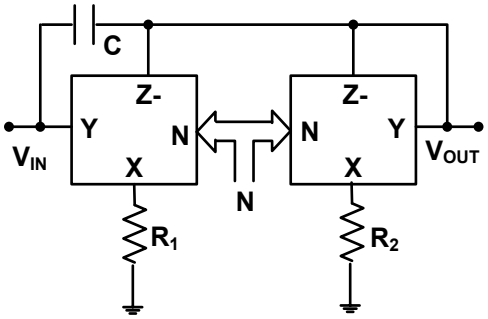

Figure 2(a). The reconfigurable phase shifter-I

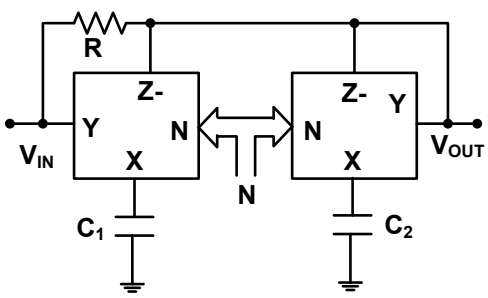

Figure 2(b). The reconfigurable phase shifter-II

With $R_1 = R_2 = R$, the phase shift angle

$$\phi = \pi - 2\tan^{-1}(\frac{\omega RC}{N}) \tag{4}$$

Similarly, the voltage transfers function for the reconfigurable phase shifter-II of "Figure 2(b)" can be expressed as

$$\frac{V_{OUT}}{V_{IN}} = -\frac{C_1}{C_2} \times \frac{S - \frac{1}{NRC_1}}{S + \frac{1}{NRC_2}} \tag{5}$$

With $C_1 = C_2 = C$, the phase shift angle

$$\phi = -2\tan^{-1}(\omega RCN) \tag{6}$$

It is thus evident from equations (4) and (6) that the phase angle between output and input of the two phase shifters can be controlled with the digital control word N.

3. The Effect of Non-Idealities

Taking the non-idealities of CCIIs into account, the relationship of the terminal voltages and currents can be rewritten as:

$$V_X = \beta_k V_Y, I_{Z-} = -\alpha_k I_X \tag{7}$$

Where, in equation (7) β_k is the voltage transfer gain from terminal-Y to terminal-X for the kth CCII and α_k is the current transfer gains for kth CCII from X to Z- respectively. Using equation (7) the ideal transfer functions and the phase angles given in (3), (4) and (5), (6) respectively for the circuit of" Figure 1(a)" and "Figure 1(b)", yields the non-ideal transfer functions and the phase shifts as follows.

$$\frac{V_{OUT}}{V_{IN}} = \left[\frac{S - \frac{\alpha_1 \beta_1 N}{RC}}{S + \frac{\alpha_2 \beta_2 N}{RC}} \right] \quad (8)$$

With $\alpha 1 = \alpha 2 = \alpha$ and $\beta 1 = \beta 2 = \beta$

$$\phi = \pi - 2\tan^{-1}\left(\frac{\omega RC}{\alpha \beta N}\right) \quad (9)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\alpha_1 \beta_1}{\alpha_2 \beta_2} \left[\frac{S - \frac{1}{\alpha_1 \beta_1 RCN}}{S + \frac{1}{\alpha_2 \beta_2 RCN}} \right] \quad (10)$$

Again with $\alpha_1 = \alpha_2 = \alpha$ and $\beta_1 = \beta_2 = \beta$

$$\phi = -2\tan^{-1}(\alpha \beta \omega RCN) \quad (11)$$

From equations (8) through (11) it is evident that the phase angles are affected slightly due to the non idealities.

4. Design and Verification

The realized digitally controlled current mode first order phase shifter of "Figure 2(a)", was designed and verified by performing PSPICE simulation with supply voltage ± 0.75V using CMOS TSMC 0.25µm technology parameters. The CMOS DPCCII with 4-bit current summing network at port-Z- of "Figure 1(b)" was used. The aspect ratios used are given in the Table 1. Initially the phase shifter was designed for a phase angle $\phi = 29^0$ at a constant frequency f_0 = 100 KHz with N = 1. Assuming C= 1nF, equation (4) yields R = 6.36KΩ. Then the phase angle ϕ was controlled through digital control word N. The variation of observed and the theoretical phase angles with different control words 'N' at f_0 = 100KHz are given in "Figure 3". The transfer gain and the input, output wave shapes at N = 4 are shown in "Figure 4". The variation of phase angle with frequency at different digital control word 'N' is shown in "Figure 5". Thus the results of "Figure 3" through "Figure 5" clearly confirm the close conformity with the theory.

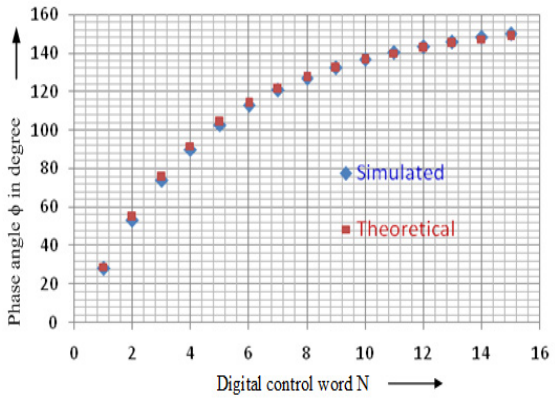

Figure 3. Phase angle variation with digital control word N at a constant frequency f_0 = 100 KHz

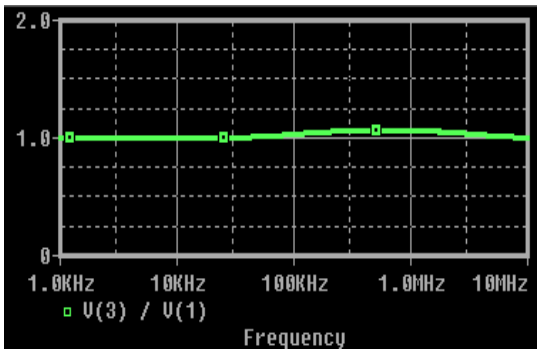

Figure 4(a). Gain Vs frequency response of the DCPS1 at N = 4

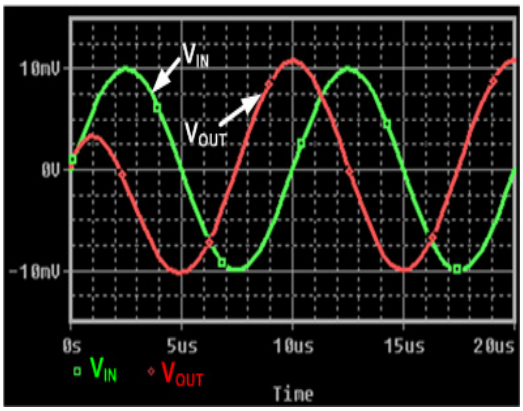

Figure 4(b). The input VIN and output VOUT wave shapes at f = 100KHz and N = 4

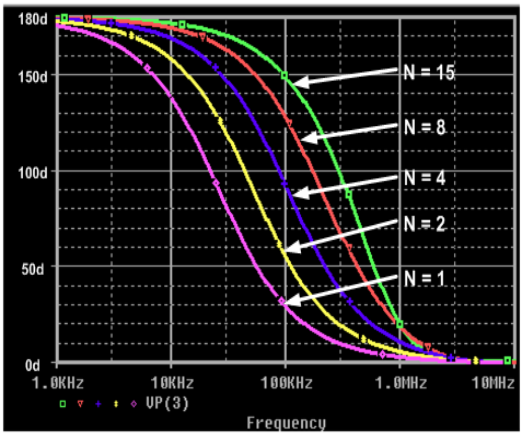

Figure 5. The phase vs frequency response at different digital control word N

Table 1. The aspect ratios of the MOSFETs of the DPCCII

MOSFETs	W µm	L µm
M_1, M_2, M_5, M_6	5	0.25
M_3, M_4, M_7, M_8	0.5	0.5
M_9, M_{10}	0.5	0.25
$M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{23}, M_{27}, M_{31}$	25	0.25
$M_{20}, M_{24}, M_{28}, M_{32}$	50	0.25
$M_{21}, M_{25}, M_{29}, M_{33}$	100	0.25
$M_{22}, M_{26}, M_{30}, M_{34}$	200	0.25

5. Conclusions

Two new voltage mode digitally controlled first order phase shifters have been realized using low voltage digitally controlled CMOS current conveyors. Each of the realized phase shifters uses two digitally controlled current conveyers along with three passive elements. The realized phase shifters provide digital control to phase angle through an n-bit control word. The realized digitally controlled continuous time phase shifters were designed and verified using PSPICE and the results thus obtained justify the theory.

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