Out-Band Interference Rejection in UWB LNA Receiver Using Coupled Inductors in Front End LNA

Hossein Rezaei[*], Ebrahim Abiri, Mohammad Reza Salehi

Department of Electrical and Electronics Engineering, Shiraz University of Technology, Shiraz, Iran

Abstract   In this paper, an ultra wide band (UWB) low noise amplifier (LNA) circuit with a new input stage is proposed. In this scheme, a combination of coupled inductors in the input stage is utilized. The input stage is able to easily reject out-band interference. This input stage is applied in an LNA with 0.18 μm technology. The LNA has a peak gain of 21.72 dB in 3.1-10.6 GHz frequency band while showing a minimum noise figure of 1.85 dB in the mentioned frequency band. This circuit rejects 15.2 dB out-band interference, while power consumption of the UWB LNA core is 11.8 mW DC which is supplied from a 1.8 V power supply. s_{11} is less than -10.3 dB over the entire bandwidth since the worst value of IIP3 over the entire bandwidth is -13 dBm, which occurs at the frequency of 10.6 GHz.

Keywords   Out-band Interference, Ultra Wide Band (UWB), Low Noise Amplifier (LNA), Coupled Inductors

1. Introduction

UWB standard was proposed by the federal communication committee (FCC)[1] in frequency range of 3.1-10.6 GHz. Due to the wide frequency band, UWB systems are capable of increasing the transmission rate up to 450 Mbps[2, 3]. Therefore, UWB systems are widely used for numerous applications in the form of WPAN[4] and short-range wireless communications[5, 6].

One of the major challenges associated with these systems is the presence of interferer signals in the mentioned frequency range which can cause destructive effects on received UWB signal. Interferer signals can be classified into two general categories. The first category mainly causes in-band interference and is a result of WLAN systems which works under IEEE 802.11a standard and takes in the frequency range of 5-6 GHz. The other category is related to WLAN systems working under IEEE 802.11 b/g standard. This kind of interference is called out-band interference, due to occupying the frequency band of 2.4-2.48 GHz. The high power interference signal caused by these systems may saturate the UWB LNA receivers and consequently degrade the sensitivity of the system. Thus, removing this type of interference is considered as a crucial issue in designing RF transceivers. As a result, the performance of UWB transceivers can be guaranteed by more than 15 dB rejection.

Lots of attempts have been carried out to improve the system performance which led to proposing various techniques. G_m-boosting[7] and thermal noise cancellation for decreasing the noise figure[8, 9], current reuse topology to perform UWB input matching and cascade amplifier with resonant load to enhance gain and reverse isolation [10], the bridged-shunt-series peaking technique for increasing the bandwidth and improving the matching in the output[11] are some of the generic methods mentioned in the literature. Although improving system performance, these methods are not capable of interference rejection. Recently, various methods have been proposed for interference rejection mostly designed using notch filters[12-15]. These filters are able to be tuned over the rejected frequency. However, because of using an additional circuit for rejecting the considered frequency, these filters will cause an increase in the power consumption and noise figure.

In this paper, we aim to reject out-band interferer signals in the input stage in such a way that there will be no increase in power consumption and no effect on the noise figure. Also, powerful tuning over the considered frequency will be preserved. Here, it is possible to increase the signal power in the next stages in an appropriate manner so that the presence of interferer signals will not be considerable.

The proposed circuit as an input stage has a maximum noise figure of 0.42 dB in the frequency range of 3.1-10.6 GHz. For both mentioned frequency bands, s_{11} and s_{22} are below -12 dB and -10 dB, respectively. The minimum gain value over the mentioned frequency band for the circuit is -0.76 dB, while the power consumption is zero, and hence CS LNA is added to the input stage to improve the gain. In order to compensate the NF of the circuit, the advantages of thermal noise cancellation techniques have been used in the second stage[8]. Furthermore, in order to improve the gain and input matching of the circuit in higher frequencies, a

new innovating technique is employed based on the bridged-shunt-series peaking method[11] in the output buffer using monolithic transformers[16].

The rest of this paper is organized as follows. In section 2, the overall circuit design, initially proposed input stage, CS LNA and output buffer with the innovative technique are presented. Simulation results are given in section 3. Finally, we will conclude the paper in section 4.

2. Circuit Design

2.1. Input Stage

The proposed input stage is shown in Figure 1. In this circuit, combination of coupled inductors with M_1 rejects out-band interference. Small signal equivalent circuit is shown in Figure 2.
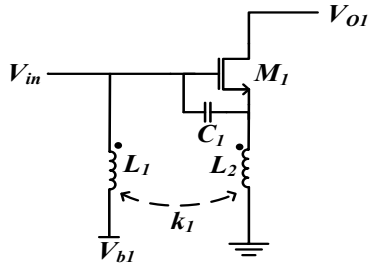

Figure 1. Schematic of the proposed interference rejection circuit
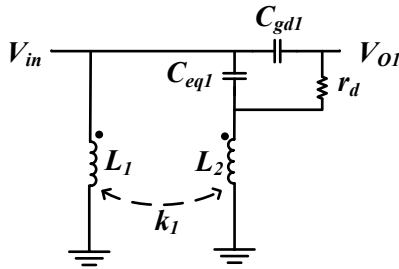

Figure 2. Small circuit equivalent of the interference rejection circuit

It is assumed that $L_2 - M \cong L_{eq}^2 / L_1$, hence, power gain can be derived as:

$$A_v = \frac{V_{O1}}{V_{in}} = \frac{\left(1 + (L_2 - M)C_{eq1}S^2\right)\left(M + r_d L_1 C_{gd1}S\right)}{L_{eq1}^2 C_{eq1} C_{gd1} r_d S^3 + L_{eq1}^2 C_{eq1} S^2 + r_d L_1 C_{gd1} S + L_1} \quad (1)$$

where $M = k_1\sqrt{L_1 L_2}$, $L_{eq1}^2 = L_1 L_2 - M'^2$ and also $C_{eq1} = C_{gs1} + C_1$. From (1), it can be deduced that there is one frequency, f, which leads gain of circuit to zero. This frequency is given in (2). Hence, the out-band interference can be rejected by tuning f on 2.4 GHz.

$$f = \frac{1}{2\pi\sqrt{(L_2 - M)C_{eq1}}} \quad (2)$$

Figure 3.a shows the gain and noise figure of the proposed circuit. s_{11} and s_{22} are illustrated in Figure 3.b. Tuneable interference rejection is achieved using different values of circuit elements in (2). Figure 4 shows simulated NF with variation of k_1.

2.2. CS LNA

In this design, the procedure of designing UWB LNA with interference rejection consists of three steps. First, as described previously, in order to reject any arbitrary frequency, the best parameter of (2) should be selected. Second, CS LNA and output buffer are added to the circuit. Third, by selecting the best value of other circuit parameters, NF, s_{11}, and s_{22} can be optimized.

Gain deficiency is the reason for designing the next stage as an amplifier. For this purpose as shown in Figure 5, CS LNA with thermal noise cancelation technique has been applied. The concept of noise cancellation can be extended as[8, 9].
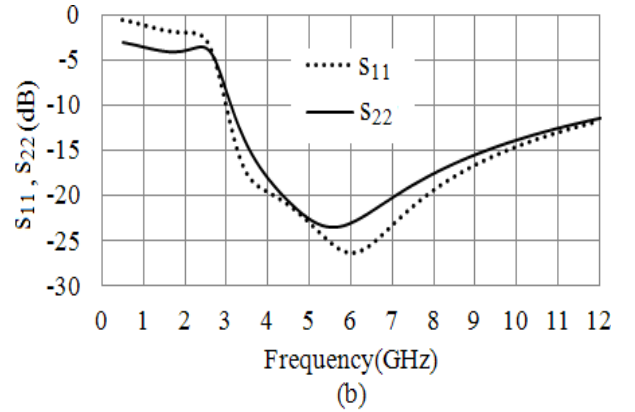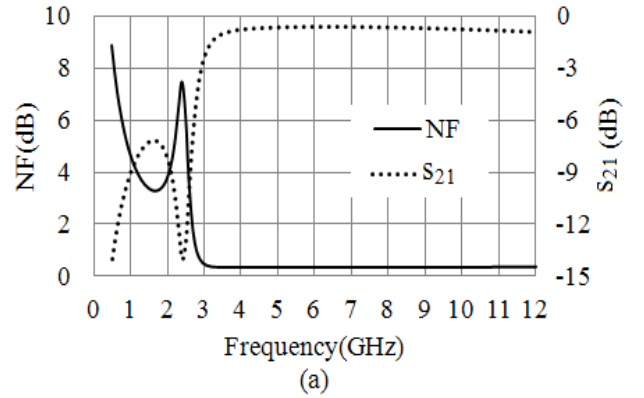

(a)

(b)

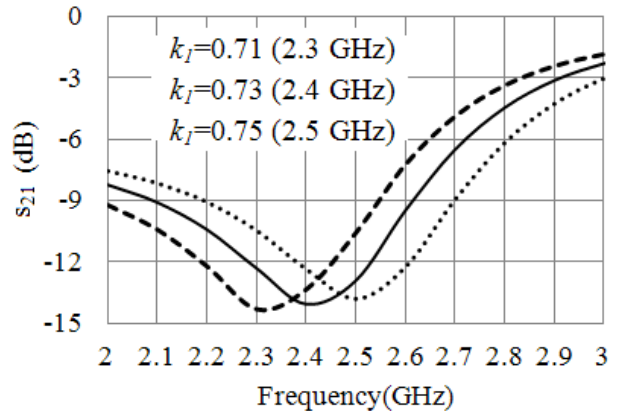**Figure 3.** a. The gain and NF b. s_{11} and s_{22} of the circuit

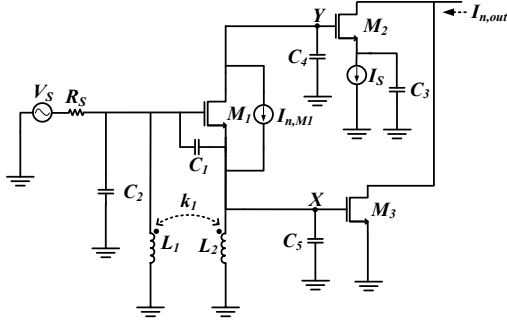**Figure 4.** NF with variation of k_1

Figure 5. Schematic design of noise cancelation technique

Since noise current of M_1 flow out of node Y and into node X, two obtained voltage noises are of different phases. These noise voltages are amplified by M_2 and M_3 which are two signal paths from M_1 in this technique. Therefore, two noise voltages are collected with each other at the output and cancel noise contribution of M_1. After cancelling the noise of M_1, the main sources of noise are M_2 and M_3. Noise calculation method in [7] is used to derive the noise contribution of M_2 and M_3 as:

$$F_{M2} = \frac{\gamma}{\alpha} g_{m2} R_S \times |H(s)|^2 \tag{3}$$

$$F_{M3} = \frac{\gamma}{\alpha} g_{m3} R_S \times |H(s)|^2 \tag{4}$$

$$H(s) = \frac{C'C_{gs3}L_{eq1}^2 s^4 + C''yI_{eq1}^2 s^3 + \left(L_{eq2}C' + L_2C_{gs3}\right)s^2 + L_1 ys + 1}{\frac{C_{gd1}}{C_{gd1}+C_{gs2}}\left(s^3 C''L_{eq1}^2 + L_1 s\right)g_{m2} + \left(s^3 C'L_{eq1}^2 + Ms\right)g_{m3}} \tag{5}$$

where $C' = C_1 + C_{gs1}$, $C'' = C' + C_{gs3}$, $L_{eq1}^2 = L_1 L_2 - M^2$, $L_{eq2} = L_1 + L_2 - 2M$, $y = 1/R_S + \left(C_2 + C_{gd1} \| C_{gs2}\right)s$
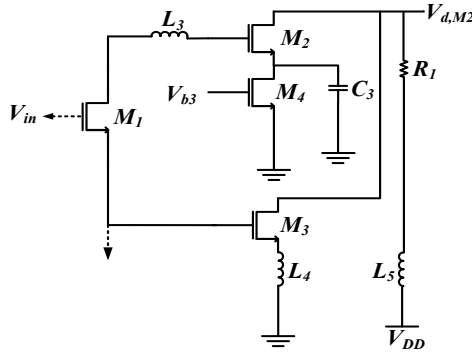

Figure 6. Schematic design of the second stage in the proposed LNA

and γ is a noise parameter, $\alpha = g_m / g_{d0}$ at which g_{d0} is the channel conductance for V_{DS}=0. As shown, by increasing g_{m2} to be more than g_{m3}, the noise factor of M_2 and M_3 can be decreased. Furthermore, increasing g_{m2} in an excessive manner can ruin power gain and NF, hence $I_{d,M2}$=4.87 mA and $I_{d,M3}$=1.69 mA are selected. As shown in Figure 5, C_2 increases the amount of C_{gd1} which improves input matching at high frequencies. On the other hand, in order to improve input matching of the circuit in high-band frequency, $C_2 \approx 1/\omega_U R$ has been used at which ω_U is the upper cut-off frequency and R (50Ω) is characteristic impedance at both ports. As shown in Figure 6, the bandwidth extension of

LNA can be obtained using inductance L_5 without any high Q requirement[17]. As shown, M_4 with gate bias provides the DC current path of M_2, since C_3 provides ac ground of circuit over working frequency bands. Resonating L_3 with input parasitic capacitance of M_2, improve input matching and gain at high frequencies.

2.3. Output Buffer

Combination of inductance L_7 and L_8 with the series inductance L_6 results in the bridged-shunt series peaking network, which further extends the bandwidth and as a consequence gain flatness will be achieved (Figure 7)[11]. It is possible to increase the signal power by using positive feedback in this scheme.

The positive gain between drain and gate can also be implemented through the use of on-chip transformer[7]. A monolithic transformer comprises two square spiral inductors. Furthermore, this transformer occupies less die area and provides a higher quality factor than two independent inductors[16]. Voltage gain in Figure 7 can be expressed as (6). A_1 can be derived as illustrated in (7).

$$Av = A_1 \times \frac{Z_L}{Z_L + L_8 S} \tag{6}$$

where in (7), $M' = k_2 \sqrt{L_6 L_7}$, $L_{eq2}^2 = L_6 L_7 - M'^2$ and $a = R_G(C_{gd5}L'' + C_{gs5}L_6) + R_2 L_6 C_{gd5}(1 + g_{m5}R_G)$. Input and output impedances are derived as in (8) and (9), respectively, where $Z_1 = R_G / (1 + j\omega R_G C_{gs5})$ and $Z_2 = r_o L_8 / (r_o + j\omega L_8)$.

Considering (7), (8) and (9), it is obvious that coupling between L_6 and L_7 can significantly affect gain, input, and output reflection coefficients of LNA. Furthermore, these effects should be considered on the proposed LNA.
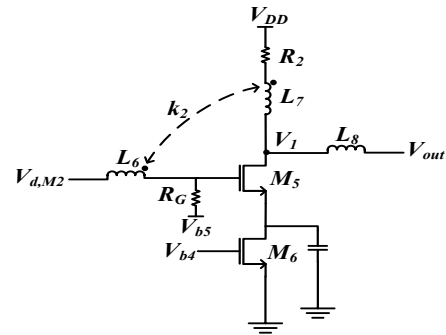

Figure 7. Schematic design of the output buffer with coupling between L_1 and L_2

$$A_1 = \frac{V_1}{V_{d,M2}} = \frac{\begin{array}{c} R_G\left[M'(C_{gs5}+C_{gd5})+L_7C_{gd5}\right]s^2 \\ +\left[M'+R_G(C_{gd5}R_2 - g_{m5}L_7)\right]s - g_{m5}R_2 R_G \end{array}}{\begin{array}{c} C_{gs5}C_{gd5}R_G L_{eq2}^2 s^4 + R_G(L_6 R_2 C_{gs5} + g_{m5}L_{eq2}^2) + L_{eq2}^2 C_{gd5}s^3 + as^2 \\ +\left[L_6 + R_G(R_2 C_{gd5} - M'g_{m5})\right]s + R_G \end{array}} \tag{7}$$

$$Z_{in} = j\omega L_6 + Z_1 + \frac{M'\omega^2(M' + g_{m5}Z_1 Z_2)}{R_2 + j\omega(L_7 + Z_2)} \tag{8}$$

$$Z_{out} = j\omega L_8 + \frac{r_o\left[\begin{array}{c} Z_1 R_2 + \omega^2(M'^2 - L_6 L_7) \\ +j\omega(R_2 L_6 + L_7 Z_1) \end{array}\right]}{r_o\left[Z_1 + j\omega(L_6 - M'Z_1 g_{m5})\right]} + Z_1 R_2 + \omega^2(M'^2 - L_6 L_7) + j\omega(R_2 L_6 + L_7 Z_1) \tag{9}$$
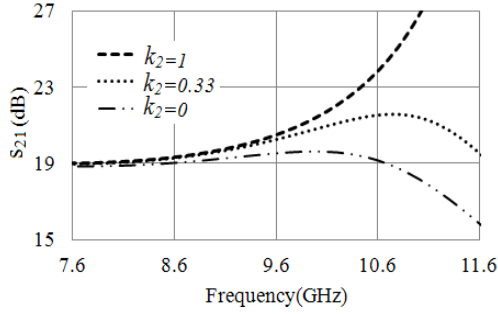
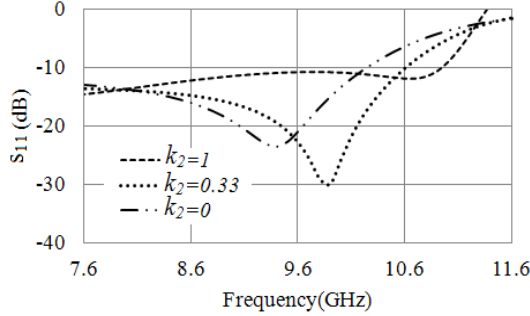**Figure 8.** The power gain versus k_2

Figure 9. The input reflection coefficient versus k_2
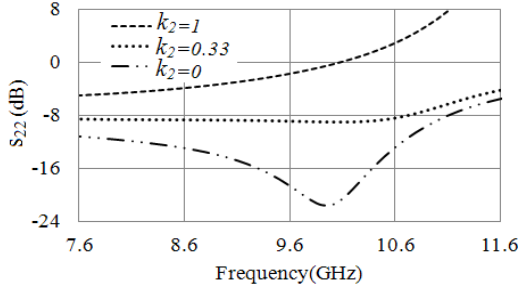

Figure 10. The output reflection coefficient versus k_2

Simulation results show that an approximate 4.7 dB increase in gain at high frequency is achieved by varying k_2 from zero to one (Figure 8). Furthermore, Figure 9 shows that this technique can bring about more than 5.5 dB improvement in s_{11} of the proposed LNA at 10.6 GHz. Unfortunately, increasing k_2 has undesirable effects on output impedance and causes about 10 dB increase in s_{22} at 10.6 GHz (Figure 10). Therefore, the optimum value of k_2 should

be chosen as 0.33 to keep s_{11} less than -10.3 dB over the entire bandwidth. Consequently, this choice leads to a power gain increase of about 2.45 dB.

3. Simulation Results

The proposed three stage UWB LNA is shown in Figure 11. The circuit has been designed with TSMC 0.18 µm CMOS technology. The simulation results are obtained using Agilent ADS 2008A simulator. All inductors are spiral with low quality factor due to high series resistances. The, first, second and third stages as an output buffer draw 0, 6.55, and 4.42 mA, respectively, from a 1.8 V power supply. Consequently, the total power consumption is 19.76 mW. Figure 12 shows the simulated noise figure of the LNA, which varies from 1.85 dB to 3.33 dB, and also has an average amount of 2.16 dB over 3.1-10.6 GHz. As shown, the variation of the circuit gain over the mentioned frequency range will be from 19 dB to 21.72 dB. Also, the average amount of power gain is 20 dB. As can be observed, 15.2 dB rejection at 2.4 GHz compared to the maximum gain is obtained. Input reflection coefficient is shown in Figure 13, which varies from -27.5 dB to the worst case of -10.3 dB. This figure also shows reverse isolation which is less than -26.5 dB over the entire working bandwidth. Output reflection coefficient (s_{22}) varies from -10 dB to the worst value of -7 dB over the mentioned frequency band.

Another parameter which should be considered is group delay since a large amount of it may distort the signal phase. In our circuit, variation of group delay ranges from 77.3 ps to 329 ps over the frequency band which is acceptable[18]. The stability factor of the proposed circuit is more than one, so UWB LNA is always stable. By applying two tones with 1 MHz spacing, the simulated IIP3 is -10.5±2.5 dBm over the mentioned frequency bandwidth.

Table 1 summarizes the performance of the recently reported UWB LNA with interference rejection using 0.18 µm CMOS technology. It is obvious that this design has the lowest amount of noise figure and the highest gain. In addition, more robust out-band interference rejection is achieved compared to the recently published CMOS LNA.

Table 1. Comparison between proposed UWB LNA with other traditional techniques

| Ref.	BW (GHz)	MAX s_{21} (dB) (average)	MAX Interference Rejection(dB)	NF_{min} (dB) (average)	s_{11} (dB)	P (mW)	IIP3 (dBm)	CMOS Technology	Interference Rejection
[12]	2-11	(16.5)	44.8@5.81GHz	2.2	<-12	16.5	NA	90-nm	Tunable active inductors
[13]	3.1-10.6	13.2	8.2@5.2GHz	4.5	<-9.5	23	-1.4	0.18-µm	Tunable notch filter
[14]	3-4.8	15	45@5.2GHz 48@2.4GHz	3.5	<-10	5*	NA	0.18-µm	Notch filter (active inductor)
[15]	1.2-9.5	14.7	35.7@5.8GHz	5.3	<-10	16	-2.5	0.18-µm	Notch filter
This work	3.1-10.6	21.72 (20)	15.2@2.4GHz	1.85 (2.16)	<-10.3	11.8*	-8@6-8 GHz	0.18-µm	Coupled inductors

* Only core LNA
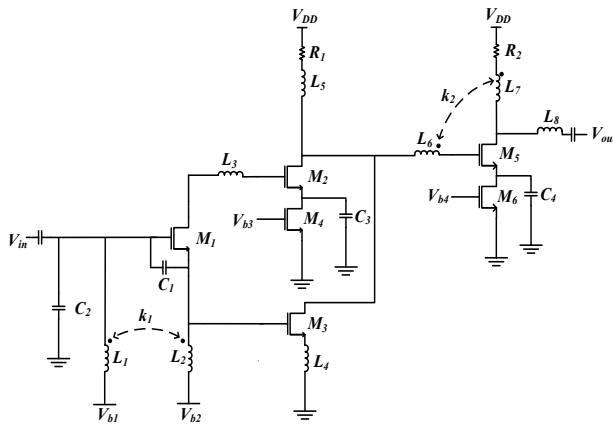
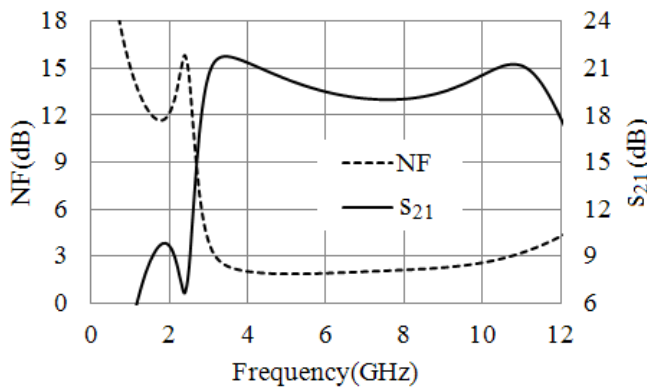**Figure 11.** Circuit diagram of the proposed UWB LNA

Figure 12. NF and gain of the circuit
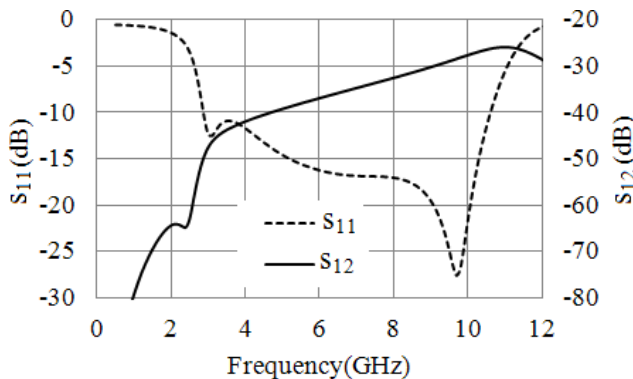

Figure 13. The input matching parameter and the reverse isolation

4. Conclusions

Interference is considered as the main challenge in the UWB LNA receivers. In order to eliminate interferences, a new technique is introduced based on coupled inductors with confident rejection of out-band interference.

Robust tuning, low noise figure and also no DC power consumption are obtained using this technique. A UWB LNA with this technique in first stage was designed. Advantages of CS LNA as an amplifier with thermal noise cancelation technique are used in the second stage of UWB LNA. Finally, output buffer is implemented with the bridged-shunt-series peaking technique to extend the band-

width. This scheme using the innovative technique aims to improve the gain of the circuit at high frequency band. In comparison to other related conventional published methods, the proposed UWB LNA exhibits the lowest noise figure over a 3.1-10.6 GHz bandwidth with the highest average power gain for UWB application in a commercial CMOS process.

REFERENCES

[1]   Federal Communications Commission (FCC), " Revision of Part 15 of the Commission's Rules, Regarding Ul-tra-Wideband Transmission," ET Docket 98-153, FCC 02-48, Released: April 22, 2002.

[2]   H. Arslan, Z. N. Chen, and M.-G. Di Benedetto, Ultra Wideband Wireless Communication, New York: Wiley, 2006.

[3]   A. Safarian and P. Heydari, Silicon-Based RF Front-Ends for Ultra Wideband Radios (Analog Circuits and Signal Processing), Springer, 2010.

[4]   H. Nikookar and R. Prasad, Introduction to Ultra Wideband for Wireless Communications (Signals and Communication Technology), Springer, 2010.

[5]   A. Khemphilal and S. Promwong, "Ultra Wideband Network in Short-Range Wireless System for Personal Computer," International Symposium on Communications and Information Technologies, pp. 1221-1224, Oct. 2006.

[6]   R. Kraemer and M. Katz, Short-Range Wireless Communications: Emerging Technologies and Applications, Wiley, 1 edition: 2009.

[7]   X. Li, "Low noise design techniques for radio frequency integrated circuits," Ph.D. dissertation, Univ. Washington, pp. 51-63, 2004.

[8]   F. Bruccoleri, E. A. M. Klumperink and B. Nauta, "Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling," IEEE J. of Solid-State Circuits, vol. 39, no. 2, pp. 275-282, Feb. 2004.

[9]   M. Forouzanfar, S. Naseh, "High Gain CMOS UWB LNA Employing Thermal Noise Cancellation," IEEE International Conference on Ultra-Wideband, pp.118-122, Sep. 2009.

[10] G. Sapone and G. Palmisano, "A 3–10-GHz Low-Power CMOS Low-Noise Amplifier for Ultra-Wideband Communication," IEEE Transactions on microwave theory and techniques, vol. 59, no. 3, pp. 678-686, Mar. 2011.

[11] S. Shekhar, J. S. Walling, and D. J. Allstot, "Bandwidth extension technique for CMOS amplifiers," IEEE J. Solid-State Circuits, vol. 41, no. 11, pp. 2424-2439, Nov. 2006.

[12] M. M. Reja, I. Filanovsky and K. Moez, "A Compact CMOS UWB LNA Using Tunable Active Inductors for WLAN Interference Rejection," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 281-284, May 2011.

[13] B. Park, S. Choi, and S. Hong, "A Low-Noise Amplifier With Tunable Interference Rejection for 3.1- to 10.6-GHz UWB Systems," IEEE Microwave and Wireless Components Letters, vol. 20, no. 1, pp. 40-42, Jane 2010.

[14] C. P. Liang, P. Z. Rao, T. J. Huang, and S. J. Chung, "Analysis and Design of Two Low-Power Ultra-Wideband CMOS Low-Noise Amplifiers with Out-Band Rejection," IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 2, pp. 227-286, Feb. 2010.

[15] Jui-Yi Lin and Hwann-Kaeo Chiou, "Power-Constrained Third-Order Active Notch Filter Applied in IR-LNA for UWB Standards," IEEE Transactions on Circuits and Systems—II: Express Briefs, vol. 58, no. 1, pp. 11-15, Jan. 2011.

[16] J. J. Zhou, et al., "Monolithic Transformers and Their Application in a Differential CMOS RF Low-Noise Amplifier," IEEE J. Solid-State Circuits, vol. 33, pp. 2020–2027, Dec. 1998.

[17] S. S. Mohan, M. D. M. Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," IEEE J. Solid-State Circuits, vol. 35, no. 3, pp. 346–355, Mar. 2000.

[18] Y. Gao, Y. Zheng and B.-L. Ooi, "A 0.18-μm CMOS UWB LNA with 5 GHz Interference Rejection," in IEEE Radio Frequency Integrated Circuits Symposium, pp. 47-50, 2007.