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# THD Minimization in Cascade Multi-level Inverters with a Few DC Sources and Optimum Voltage Levels

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**Abstract** Nowadays, multilevel converters are a good solution for power applications regarding the fact that they can obtain high power using mature medium-power semiconductor technology. Among three types of inverter topologies, cascaded multilevel inverter reaches the higher output voltage and power levels (13.8 kV, 30 MVA), and the higher reliability due to its modular topology. Although multi-level inverters generate low harmonic distortion, the output voltage waveform is not accurately a sinusoidal wave. Minimization of total harmonic distortion (THD) is one of the objectives of inverter field researches. On the other hand, reduction of construction costs is the other purposes of power electronics engineering issues. This could be achieved by reduction of some elements of the circuit. Therefore, this paper tries to combine two techniques in order to accomplish better cascade multi-level inverter. First technique produces more voltage steps with less number of DC sources and less number of switches. Second one tries to set the optimum values for DC sources and subsequently voltage steps through Fourier analysis. Finally, techniques would be compared.

**Keywords** Cascade Multi-Level Inverter, H-Bridge, Optimum Voltage Levels, DC Sources, Total Harmonic Distortion

## 1. Introduction

Application of power electronics in power systems are growing rapidly. In distributed generation, power electronics is needed to interface non-conventional energy sources such as wind, photovoltaic, and fuel cells to the utility grid. In photovoltaic systems, solar cells produce dc, with I-V characteristic shown in Figure 1a that requires a power electronics interface to transfer power into utility system, as shown in Figure 1b.

Use of power electronics allows control over the flow of power on transmission lines, an attribute that is especially significant in a deregulated utility environment. Also, the security and the efficiency aspects of power systems operation necessitate increased use of power electronics in utility applications [1].

The term multilevel began with the three level converters [2]. Later, several multilevel converter topologies have been developed [3–6]. In 1998 Manjrekar has proposed a cascade topology that uses multiple dc levels, which instead of being identical in value are multiples of each other [7, 8]. He also uses a combination of fundamental frequency switching for some of the levels and PWM switching for part of the levels to achieve the output voltage waveform. This approach enables a wider diversity of output voltage magnitudes; however, it also results in unequal voltage and current ratings for each of the levels and loses the advantage of being able to use identical modular units for each level.

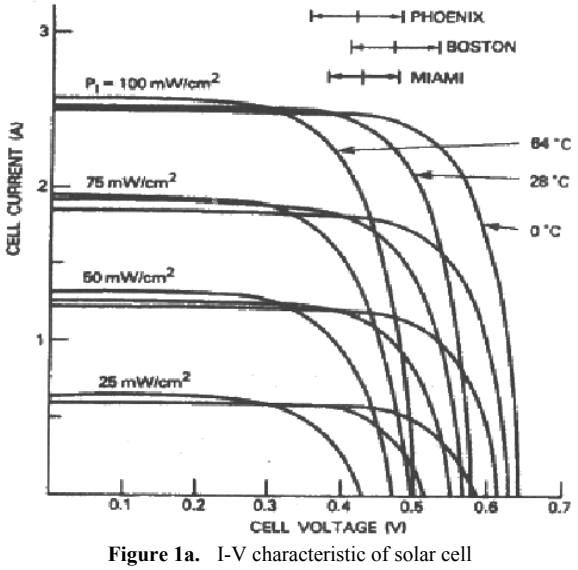


**Figure 1a.** I-V characteristic of solar cell

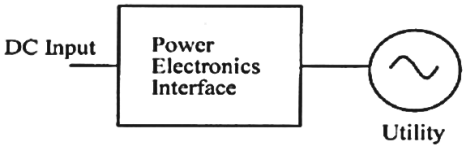


**Figure 1b.** Transferring power to utility by the means of power electronics

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The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows [9, 10].

***Advantages:***

The number of possible output voltage levels is more than twice the number of dc sources ($m = 2s + 1$).

• The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

***Disadvantages:***

• Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

## 2. First Technique: More Voltage Steps Using Less DC Sources and Switches

Each H-bridge connected to $V_{dc}$ volts DC source, could generate three voltage levels: $V_{dc}$, 0, and -$V_{dc}$. Beside, each decimal number could be converted into binary number. For instance, to count from zero to seven, 3 binary digits would be required. Below illustration shows that how a decimal number (6) is produced by three digits in binary system. Another word, below illustration shows that how a decimal voltage step (6) is produced by three DC sources.

$$(110)_2 = 1^4 1^2 0^1 = 6 \quad (1)$$

Above phrase shows that, there is no need to use six separate volatge sources to produce 6-level inverter. To produce step sixth, according to above phrase, three different voltage sources would be needed. Voltage sources should have values equal to powers of 2:

$$V_0 = 2^0 \times V_{dc} \quad (2)$$

$$V_1 = 2^1 \times V_{dc} \quad (3)$$

$$V_2 = 2^2 \times V_{dc} \quad (4)$$

To generate step sixth, the H-bridge connected to $V_0$ should produce 0 volts. The H-bridge connected to $V_1$ should produce $V_1$ volts and The H-bridge connected to $V_2$ should produce $V_2$ volts. Then the output voltage would be equal to $6\times V_{dc}$. Using this technique, $2^s - 1$ steps is produced by $s$ DC sources, as shown in Figure 2.

Another advantage of this technique is to use less switches. If the condition of a switch in a whole period doesn't change, it could be replaced with a open circuit or a short circuit (according to switch's condition). Additionally, it is possible to reduce the duty cycle of circuit by one H-bridge module. It means that, if one can produce the positive (negative) part of sinusoidal wave and apply it to the input of H-bridge module, then it is possible to generate the negative (positive) part of sinusoidal wave in the final output terminals. New form of multi-level cascade invereter for producing 3-levels is shown in Figure 3.

As it is obviuse in Figure 3, for two H-bridge configuration the number of switches doesn't change. But as the number of H-bridge blockes increases the number of switches could be decreases in comparision with standard multi-level configuration.

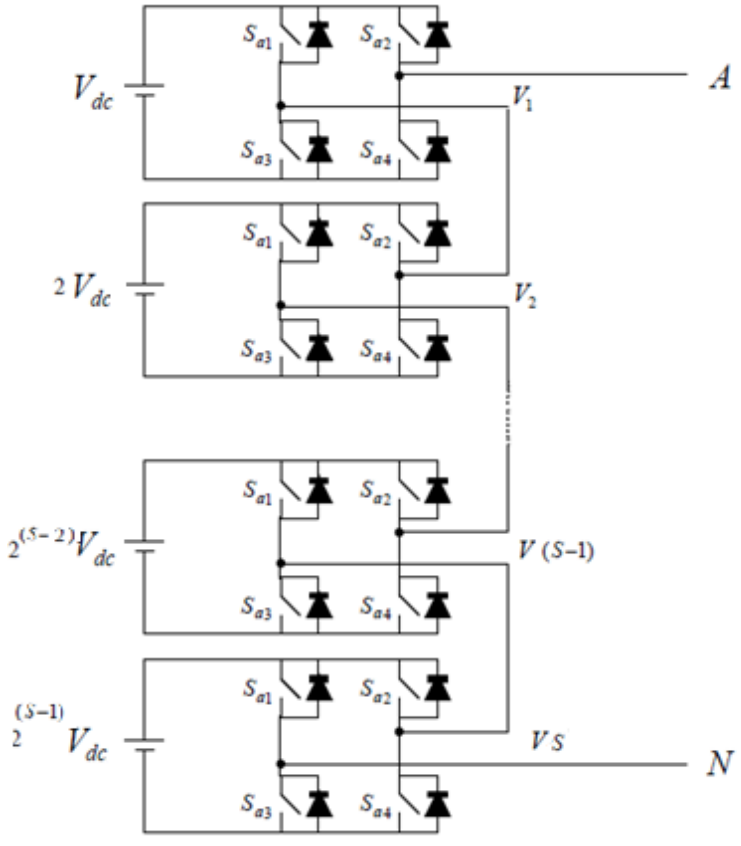



**Figure 2.** Cascade mult-level invereter with few DC sources and more voltage steps

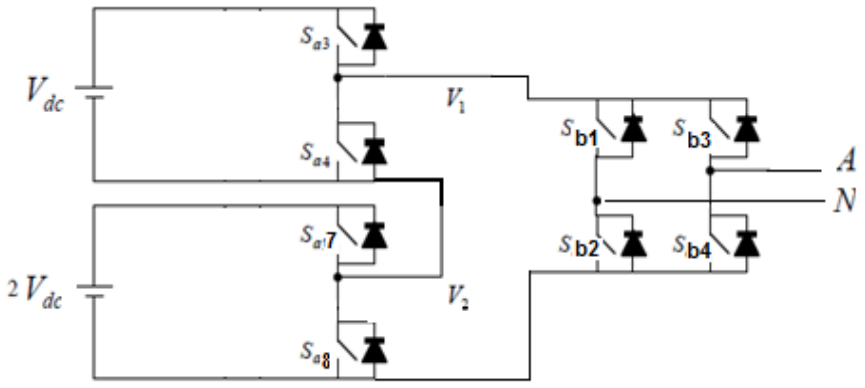



**Figure 3.** New configuration of switchecs in multi-level inverter

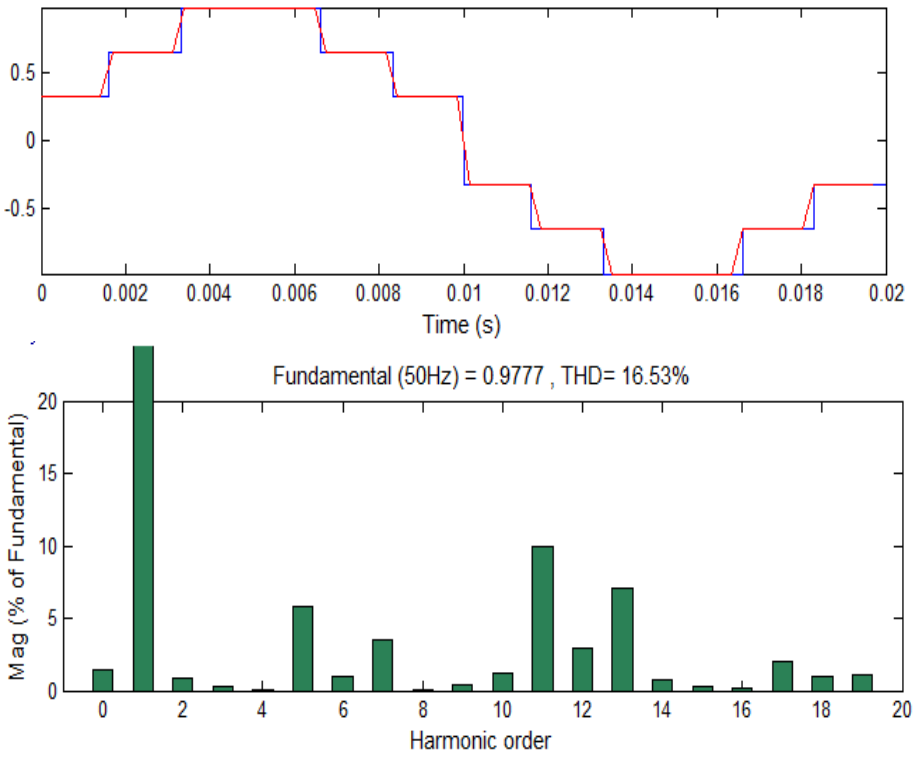
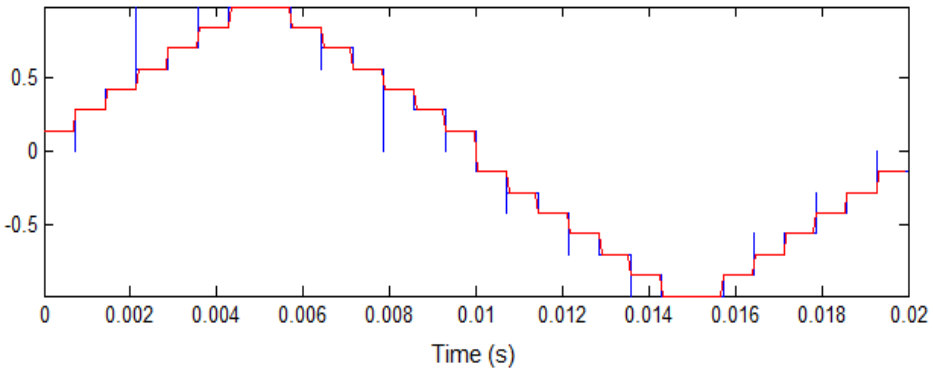



**Figure 4.** Signal and FFT analysis for 3-level inverter using only two DC sources



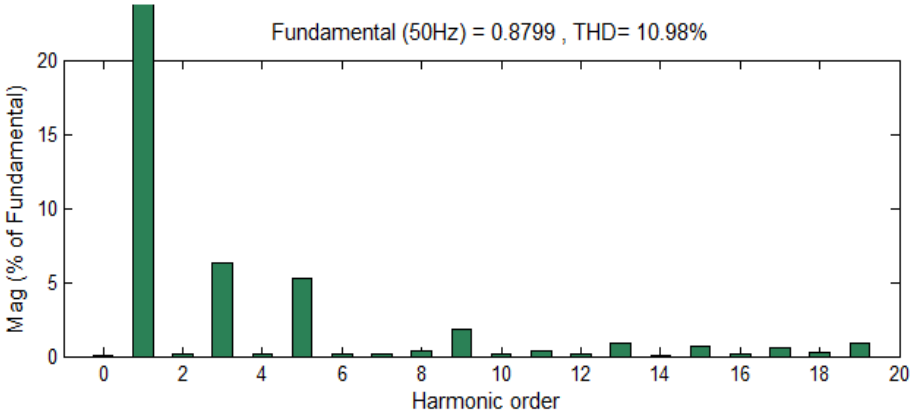



**Figure 5.** Signal and FFT analysis for 7-level inverter using only three DC sources

If $s$ stands for number of H-bridge blocks and $b$ stands for number of used switches, then:

$$\text{For standard multi-level inverter: } b = s \times 4 \quad (5)$$

$$\text{For this technique: } b = (s \times 2) + 4 \quad (6)$$

Using this technique the total harmonic distortion for three and seven steps are simulated and calculated.

Figure 4 shows that using this technique leads to produce 16.53% total harmonic distortion for 3-level inverter. Figure 7 illustrates that using only three DC source could produce 7-level inverter and it generates THD about 10.98%.

## 3. Second Technique: Optimum Voltage Levels

By writing Fourier series for the output signal of a cascade inverter one can find the harmonic orders equation. Coefficients of odd components of Fourier series are the harmonic orders. Fourier series equation is:

$$f(x) = a_0 + \sum_{n=1}^{\infty} \left( a_n \cos\frac{n\pi x}{L} + b_n \sin\frac{n\pi x}{L} \right) \quad (1)$$

Since output voltage is a sinusoidal waveform and sin function is an odd function $a_n$ is equal to zero. So $b_n$ determines the amplitude of harmonics. General shape of $b_n$ equation is:

$$b_n = \frac{1}{L}\int_{-L}^{+L} f_{(x)} sin\frac{n\pi}{L} x dx \quad (2)$$

Fourier series for the output voltage of 2-level inverter which is shown in Figure 6 has been written, the coefficient of sinusoidal components is:

$$b_n = \frac{4A}{n\pi}\left[p + (1-p)cos\frac{n\pi}{4}\right] \quad (3)$$

Where $A$ is the amplitude of fundamental sin wave or summation of DC voltage sources. $p$ is a percentage of amplitude which is occurs in first step. $p$ shows the value of first step. On the other word $p$ determines the value of first DC voltage source in a 2-level inverter. $n$ is the number of harmonic order.

For 3-level inverter $b_n$ is equal to:

$$b_n = \frac{4A}{n\pi}\left[p_0 + p_1 cos\frac{n\pi}{6} + (1-p_0-p_1)cos\frac{2n\pi}{6}\right] \quad (4)$$

Where $p_0$ and $p_1$ show the values of first and second steps, respectively.

By the help of principle of mathematical induction one can write the equation for amplitude of harmonics for k-level inverter:

$$\mathrm{b_n} = \frac{4A}{\mathrm{n\pi}}\left[\sum_{\mathrm{i=0}}^{\mathrm{K-2}} \mathrm{p_i} \cos\frac{\mathrm{in\pi}}{\mathrm{2k}} + \left(1 - \sum_{\mathrm{i=0}}^{\mathrm{K-2}} \mathrm{p_i}\right)\cos\frac{\mathrm{(k-1)n\pi}}{\mathrm{2k}}\right] \quad (5)$$

Where, $p_i$ are the values for each voltage level. The total harmonic distortion equation could be written as follows:

$$THD: \frac{\sqrt{\sum_{\mathrm{n=2}}^{\mathrm{n=\infty}} \mathrm{b_n}^2}}{\mathrm{b_1}} \quad (6)$$

Equation (5) will helps to calculate the $b_n$ values rapidly. So there is no need to write the Fourier series for finding $b_n$ values. Equations (5) and (6) help to determine the optimum value of voltage levels. To find the optimum value of levels we should answer this question:

Which values of $p_0, p_1, p_2, \ldots$ will minimize equation (6)?

It is clear that:

$$0 < p_0, p_1, p_2, \ldots < 1 \quad (7)$$

$$p_0 + p_1 + p_2 + \cdots = 1 \quad (8)$$

Objective function which should be optimum is a multi-variable function. When multi level inverter has $K$ steps the objective function has $K-1$ variables. For optimization process MATLAB software has been used. To obtain steps values, constrained nonlinear minimization method has been used. If only $b_1$, $b_3$, $b_5$, and $b_7$ have been considered, values shown in Table.1 are the optimum ones.

**Table 1.** Optimum values for voltage levels (DC sources)

| Optimum values | Number of inverter levels | | | | | |
|---|---|---|---|---|---|---|
| | 2 | 3 | 4 | 5 | 6 | 7 |
| $p_0$ | 0.414 | 0.268 | 0.199 | 0.175 | 0.153 | 0.137 |
| $p_1$ | 0.586 | 0.464 | 0.368 | 0.268 | 0.217 | 0.18 |
| $p_2$ | | 0.268 | 0.281 | 0.283 | 0.248 | 0.221 |
| $p_3$ | | | 0.152 | 0.166 | 0.184 | 0.177 |
| $p_4$ | | | | 0.108 | 0.123 | 0.132 |
| $p_5$ | | | | | 0.075 | 0.103 |
| $p_6$ | | | | | | 0.050 |

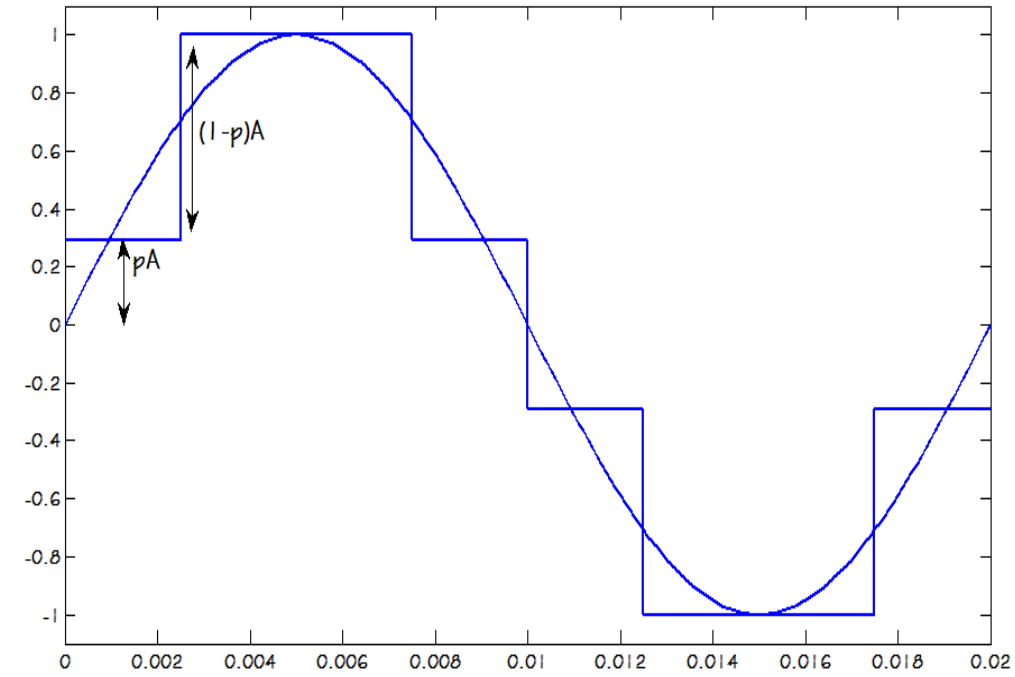



**Figure 6.** Output voltage of 2-level inverter and its fundamental sin wave

For second technique, simulation process for 3 and 7 levels have been performed. Results are shwon in figures 7 and 8. With optimum DC sources, THD decreases to 15.59% for 3-level and 7.27% for 7-level.

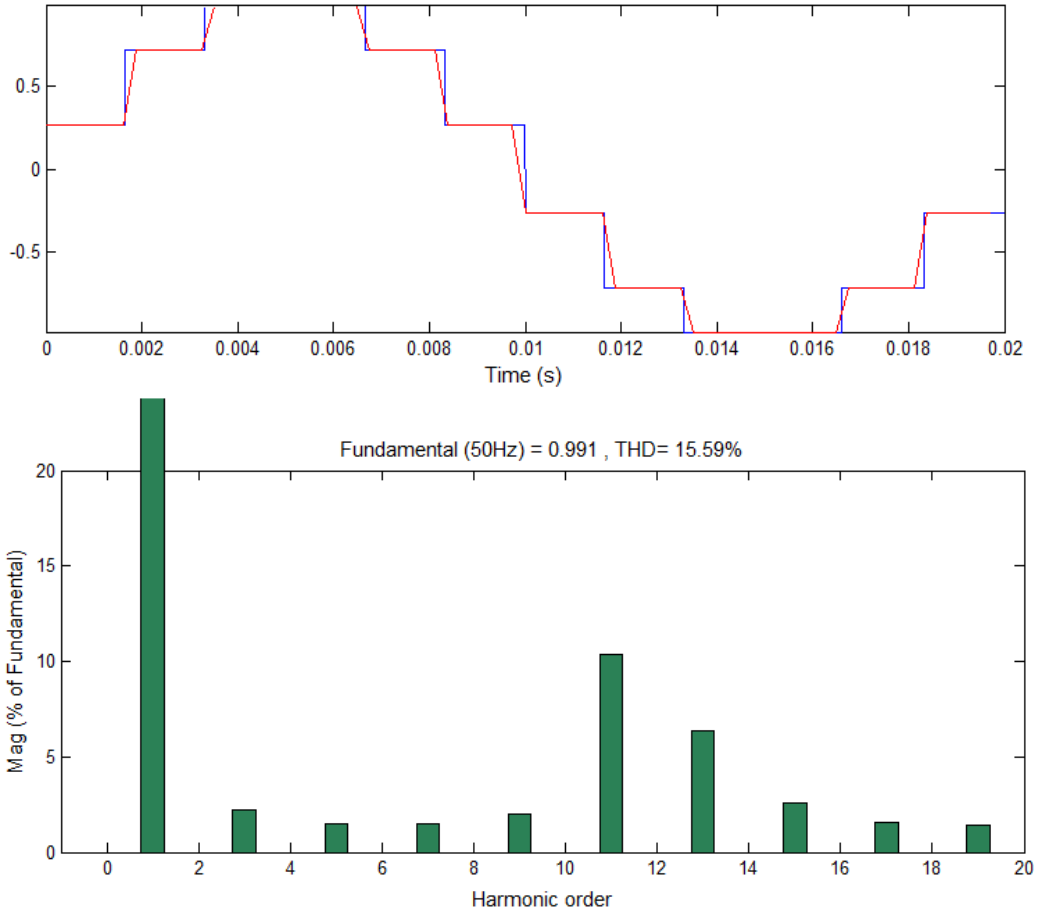



**Figure 7.** Signal and FFT analysis for 3-level inverter using optimum DC sources

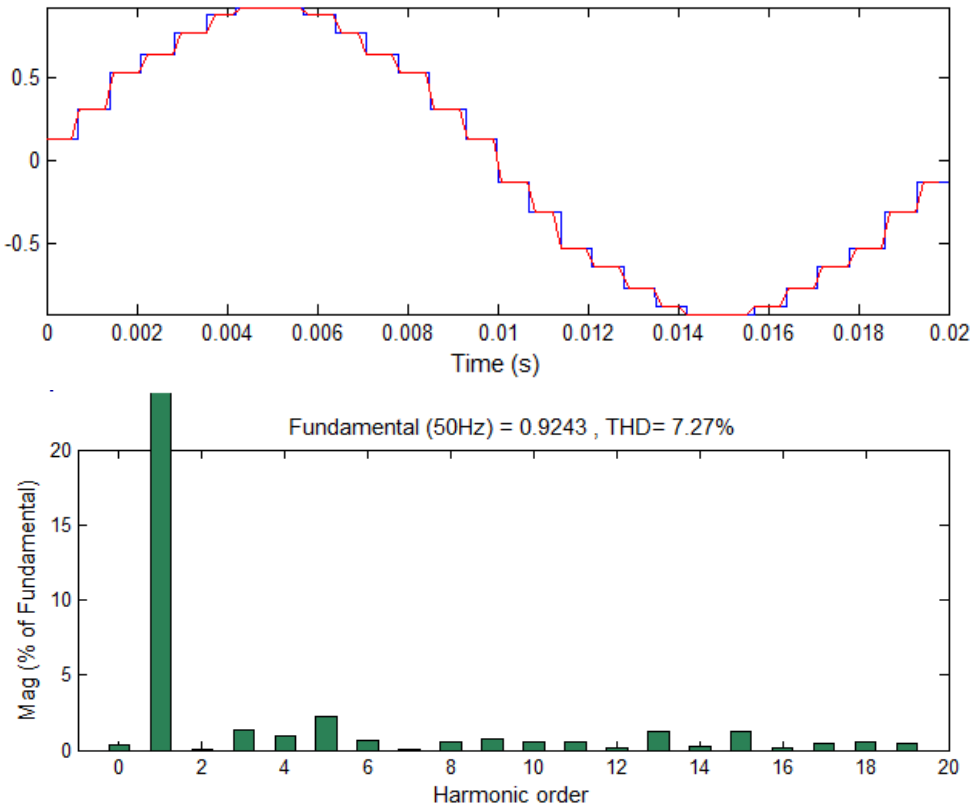



**Figure 8.** Signal and FFT analysis for 7-level inverter using optimum DC sources

## 4. Third Technique: Combination of First and Second Techniques

In order to achieve better sinusoidal wave form in the output of cascade multi-level inverter, two previous techniques are combined.Additionally, this combination technique provides low costs due to few usage of sources and swithches.

Number of DC sources determines the variables of objective function in minimization procedure. As an example, to minimize the THD in 7-level multi level, there exists three variables: V(1), V(2), and V(3). Objective function for 7-level inverter could be written as follows:

Function THD= func7(v)

b1=v(1)+(v(2)-v(1))*cos(pi/14)+v(1)*cos(2*pi/14)+(v(3)-v(2)-v(1))*cos(3*pi/14)+v(1)*cos(4*pi/14)+(v(2)-v(1))*cos(5*pi/14)+(1-v(2)-v(3))*cos(6*pi/14);

b3=(v(1)+(v(2)-v(1))*cos(3*pi/14)+v(1)*cos(6*pi/14)+(v(3)-v(2)-v(1))*cos(9*pi/14)+v(1)*cos(12*pi/14)+(v(2)-v(1))*cos(15*pi/14)+(1-v(2)-v(3))*cos(18*pi/14))/3;

b5=(v(1)+(v(2)-v(1))*cos(5*pi/14)+v(1)*cos(10*pi/14)+(v(3)-v(2)-v(1))*cos(15*pi/14)+v(1)*cos(20*pi/14)+(v(2)-v(1))*cos(25*pi/14)+(1-v(2)-v(3))*cos(30*pi/14))/5;

b7=(v(1)+(v(2)-v(1))*cos(7*pi/14)+v(1)*cos(14*pi/14)+(v(3)-v(2)-v(1))*cos(21*pi/14)+v(1)*cos(28*pi/14)+(v(2)-v(1))*cos(35*pi/14)+(1-v(2)-v(3))*cos(42*pi/14))/7;

THD=sqrt(b3^2+b5^2+b7^2)/b1;

Results of minimization for 3 and 7-level inverters shows that the optimum values of DC sources are:

For 3-level inverter: $\begin{cases} V(1) = 0.259 \\ V(2) = 0.741 \end{cases}$

For 7-level inverter: $\begin{cases} V(1) = 0.143 \\ V(2) = 0.255 \\ V(3) = 0.603 \end{cases}$

Simulation process have done by the use of this optimum values in MATLAB software. Switching frequency of combined technique is equal to: number of levels×100 Hz. Figure 9 and Figure 10 show signal and FFT analysis for combined technique.

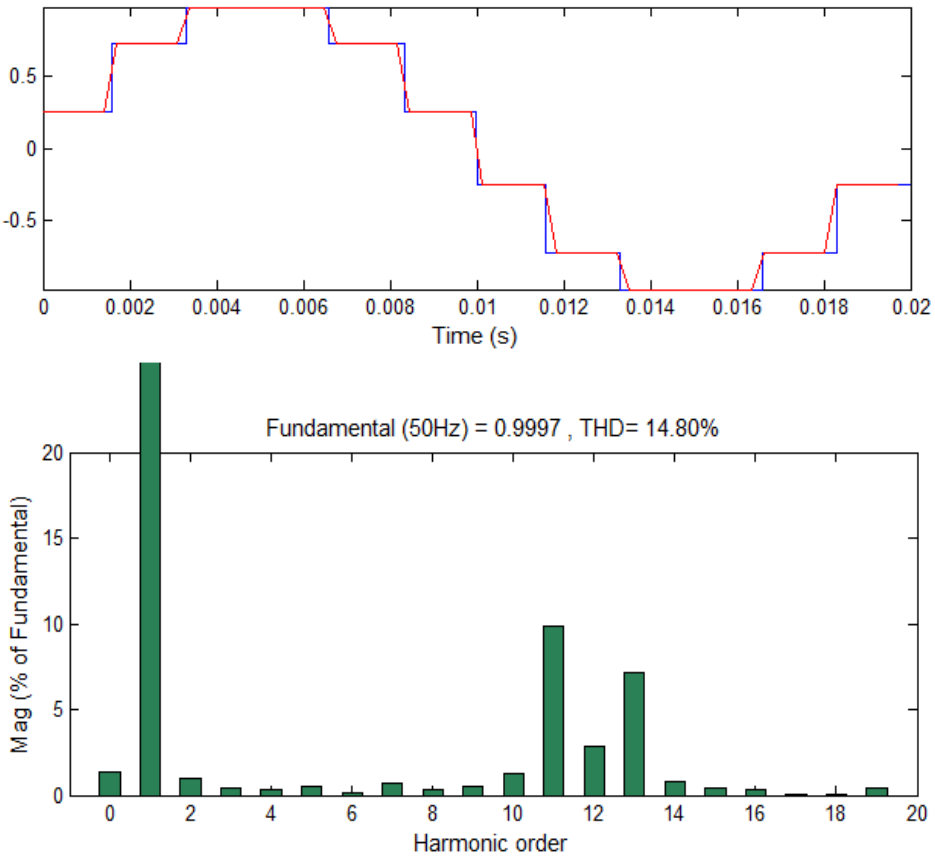



**Figure 9.** Signal and FFT analysis for 3-level inverter using combined technique

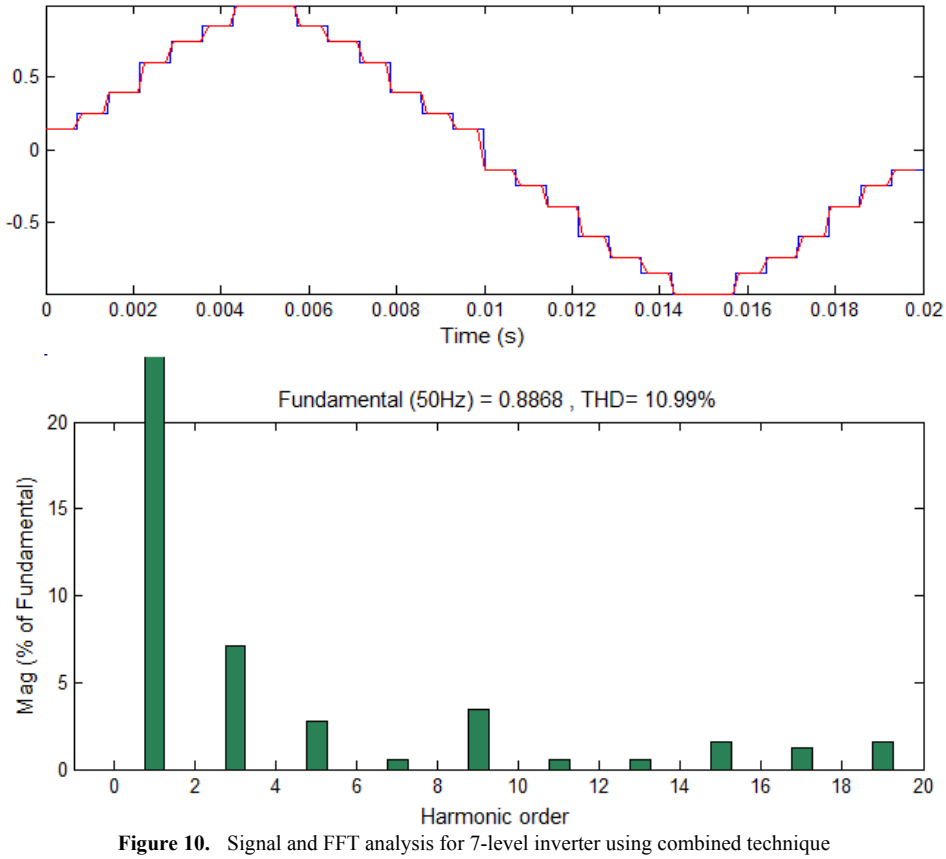



**Figure 10.** Signal and FFT analysis for 7-level inverter using combined technique

For 3-level the THD reduces about 1.73% and 0.79% in comparison to first and second techniques, respectively. THD in this case is equal to 14.80%. For 7-level THD is equal to 10.99%. this value is bigger than THD of second technique but it is approximately equal to THD of first technique.

## 5. Forth Technique: Standard Cascade Multi-Level Inveretr

This section reviews the standard multi-level inverter so as to compare with introduced techniques. In standard conventional multi-level inverter, DC sources are equal and output voltage level is the same to number of DC sources. Figure 11 shows the standard cascade multi-level inverter.

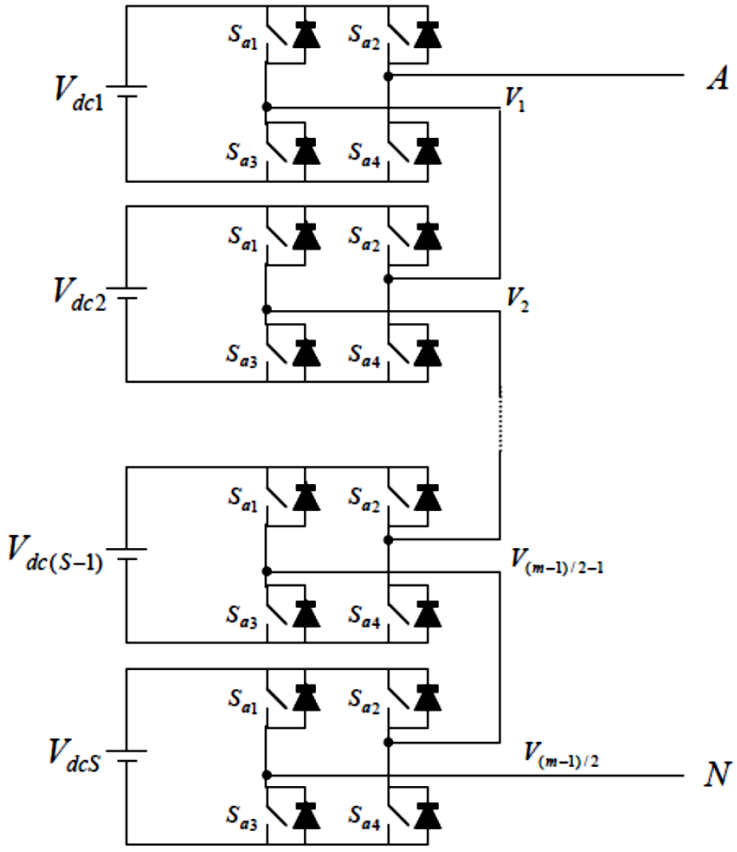
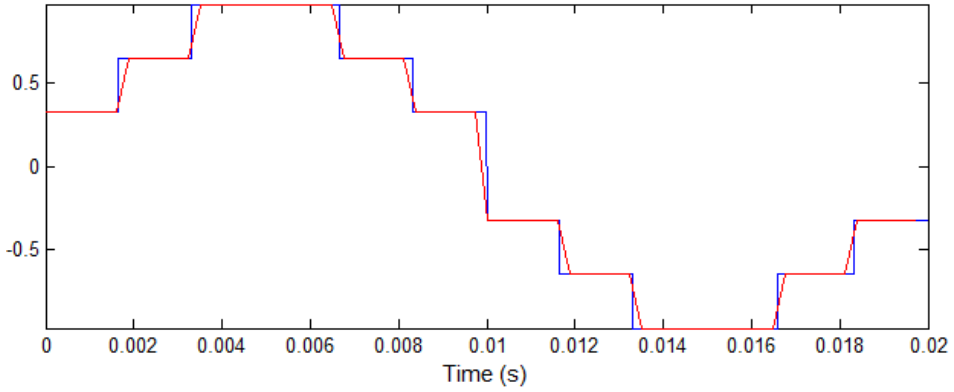



**Figure 11.** Standard cascade multi-level inverter

Signal and FFT analysis of 3 and 7-level standard multi-level has been performed and the rresults are shown in Figure 12 and 13, respectively.



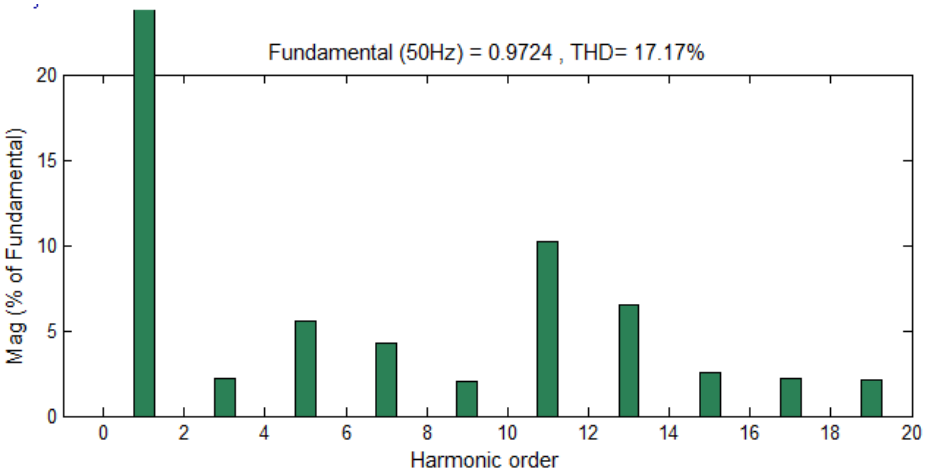



**Figure 12.** Signal and FFT analysis for 3-level inverter using standard technique

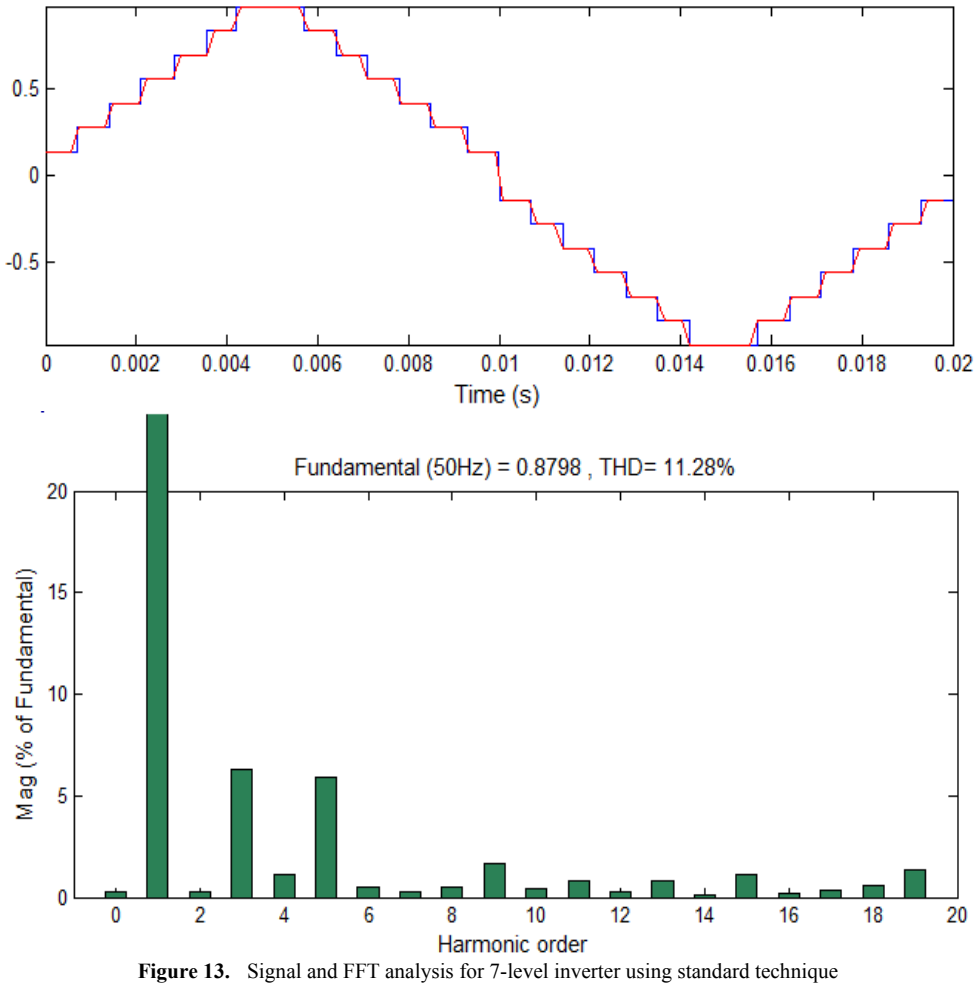



**Figure 13.** Signal and FFT analysis for 7-level inverter using standard technique

It could be seen that the THD in standard case is higher than other techniques.

## 6. Comparison

This section summerizes the features of four techniques in table.2 and table.3.

**Table 2.** THD values for differenr techniques

| THD (%) | Number of inverter levels | | | | | |
|---|---|---|---|---|---|---|
| | 2 | 3 | 4 | 5 | 6 | 7 |
| *First tech.* | 23.64 | 16.53 | 13.62 | 12.32 | 10.98 | 10.98 |
| *Second tech.* | 22.98 | 15.59 | 11.37 | 9.20 | 7.80 | 7.27 |
| *Combined tech.* | 22.33 | 14.80 | 11.87 | 11.73 | 10.90 | 10.99 |
| *Standard tech.* | 24.13 | 17.17 | 13.56 | 12.21 | 11.60 | 11.28 |

**Table 3.** Used DC sources and switches in different techniques

| Number of used DC source | Number of inverter levels | | | | | |
|---|---|---|---|---|---|---|
| | 2 | 3 | 4 | 5 | 6 | 7 |
| *First tech.* | 2 | 2 | 3 | 3 | 3 | 3 |
| *Second tech.* | 2 | 3 | 4 | 5 | 6 | 7 |
| *Combined tech.* | 2 | 2 | 3 | 3 | 3 | 3 |
| *Standard tech.* | 2 | 3 | 4 | 5 | 6 | 7 |
| Number of used switches | Number of inverter levels | | | | | |
| | 2 | 3 | 4 | 5 | 6 | 7 |
| *First tech.* | 8 | 8 | 10 | 10 | 10 | 10 |
| *Second tech.* | 8 | 12 | 16 | 20 | 24 | 28 |
| *Combined tech.* | 8 | 8 | 10 | 10 | 10 | 10 |
| *Standard tech.* | 8 | 12 | 16 | 20 | 24 | 28 |

According to table.2 second technique provides less THD than the others. Consequently, in cases that the main object is to acheive less THD, this technique should be used.

# 7. Conclusions

This paper has successfully demonstrated some techniques in cascade multi-level inverters in order to achieve low costs and less total harmonic distortion. Although combined technique provides less number of switches and DC sources but watt usage in all techniques would be equal. Another word, costs would reduce in first and combined techniques because as the power in a DC source increases, per power cost would decrease. Therefore, it is better to use a 1 watt, a 2 watts, and a 4 watts DC sources instead of using seven 1 watt DC sources. Features of combined technique could be named as follows:

1) Low construction costs

2) Less THD due to optimum DC sources

Optimum values are gained in minimization process, were not round values. Available DC sources such as photovoltaic panels have round voltage values. Thus, for practically design and built a low harmonic and low cost cascade multi-level inverter, optimum DC source values in combined technique should cut or round. This could be a part of our future works.

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