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Preface: Special Issue on Emerging Techniques for Nano-Scales CMOS Integrated Circuits Design

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Despite Challenges, CMOS Technology is here to Stay. While several promising alternatives to replace silicon based CMOS technologies are actively developed; CMOS maturity, low manufacturing cost, high speed and low power consumption will extend its dominance for at least in the next ten to fifteen years. As the CMOS technology scales down to the nanometer level IC designers are facing several challenges including supply voltage reduction, excessive leakage current and statistical uncertainty with process variations and mismatch that all restrict the design of high performance digital, analog, mixed-signal, and RF circuits. Also the growing demand for more complex ultra-low power devices exacerbates these challenges and makes the operation reliability of integrated circuits despite of variations a hard to achieve goal.

This special issue of Microelectronics and Solid State Electronics includes the topics from analog integrated circuit synthesis flow, low-power RF circuits design and modeling, single-event transient testing for integrated circuits, and wireless network-on-chip to enable communication between processing cores.

Four innovative papers were selected after rigorous review process. The first paper, by T. Liao *et al.*, describes a diverse analog integrated circuit synthesis flows to generate a quality-guaranteed tape-out CMOS designs. This paper puts emphasis on the impact of the Layout Dependent Effects (LDEs).In particular, two dominant LDEs, Well Proximity Effects (WPE) and Shallow Trench Isolation (STI) effects, are discussed along with experiments to illustrate the severity of the induced performance degradation on the next-generation analog synthesis methodologies and flows. The second paper, by H. Yu *et al.,* presents a modified ultra-compact model which is numerically accurate for nano-scale bulk-driven low voltage nano-scale CMOS circuits. Also a guideline of quantitatively analysing nano-scale CMOS circuits is established. The distortion analysis of nano-scale gates and bulk-driven amplifiers is demonstrated as an example to show the importance of the nonlinear output conductance and the cross-terms, as well as the effectiveness of the accurate ultra-compact model. The third paper, Y. Ren *et al.,* compares Single-Event Transient (SET) testing results on integrated circuits using the pulsed X-ray technique with earlier results using the heavy ion and the pulsed laser. The advantages and limitations of the pulsed X-rays as a practical method for SET investigation were presented and analysed. The results were consistent with those of the previous heavy ion and pulsed laser testing, which indicates that the pulsed X-ray technique is a complementary tool to investigate SET. The final paper, by J. Bousquet, describes a 10-Gbps wireless network-on-chip to enable communication between 256 processing cores. A cross-layer design has been discussed to reduce hardware overhead. To enable a 10-Gbps wireless network, 16 5-GHz channels are provisioned in the 300-GHz frequency range. At each core, a fully bi-directional transceiver relying on-off keying to minimize energy consumption has been described and a power budget of 11.4 mW per core has been estimated.

I would like to thank all the authors for their valuable contributions and all the reviewers for their time and efforts in helping to select the papers. I would like also to thank the Scientific & Academic Publishing supporting personnel for their expert help.

Finally, I hope that the readers of of Microelectronics and Solid State Electronics journal will enjoy reading the papers in this special issue and will find them useful in their future works on nano-scales CMOS integrated circuits design.