

# Temperature Dependence of Carbon Nanotube Field Effect Transistor under Non-Ballistic Conduction Considering Different Dielectric Materials

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**Abstract** This paper deals with a simulation model to analyse the behaviour of carbon nanotube field effect transistors (CNTFETs) under non-ballistic conditions and based on the changes of gate dielectric constant the performance of CNTFETs has been explored in detail as a function of temperature. A thorough study of the combined non-ballistic effect on the performance of CNTFETs has been conducted with different principle characteristics of CNTFETs and the output of the device has been analysed. Effects on the drain current under different temperature with different dielectric constant is observed under different gate voltages Also it has been observed that within a certain range of temperature both on-state and off-state current retains in steady state. However with a higher value of temperature and dielectric constants, on and off state current changes and as a result it degrades the current ratio. In addition, the ratio of quantum to insulator capacitance, drain-induced barrier lowering (DIBL) with respect to the changes of gate dielectric constant as a function of temperature are further investigated. Quantum capacitance increased with temperature which increases the ratio of quantum to insulator capacitance. The DIBL vary slightly with higher value dielectric material and reaches to desired ballistic condition value with an ambient temperature.

**Keywords** On-state current, Off-state current, Drain-induced barrier lowering (DIBL), Quantum Capacitance

## 1. Introduction

One of the most imaging features of carbon nanotube is its application on electronics field especially in Carbon nanotube field effect transistor (CNTFET). The motivation of research in CNFET is fuelled by the unique quasi-ideal electronic as well as optical characteristics of carbon nanotube [1, 2]. Just like MOSFET it supplies electrons from source terminal to drain terminal for collection. However, properties like higher on-state current, high channel density and high electric density makes a CNTFET superior than MOSFET [3-6]. The scaling of MOSFET's increases with the number of transistors integrated on a chip. Due to MOS scaling, capacitance of the device increased while decreasing the thickness of the oxide layer. In case of CNTFET, gate oxide thickness maintains an inverse relationship with drain current [7]. An insulator with higher dielectric constant can be the answer. For modelling a CNTFET, mesoscopic physics analysis with higher dielectric constant gives different aspects of CNTFET and their structures. Also like MOSFET, temperature will play avital role in the CNTFET

performance and characteristics [9]. Hence, various properties of CNTFET is investigate under different temperatures.

When channel length of CNT transistor has a length smaller than the carrier mean free path (MPF) but larger than the Coulomb blockade length, it shows the ballistic nature. Due to the variance of energy domain, non-ballistic transport in CNTs becomes prominent [10]. As a result, the mobility of the carrier changes due to the fluctuation of the transmission coefficient of carrier to travel through a single-defect coulomb potential channel. However, contamination, vacancies, contact to the substrate and absorbed molecules can also cause the non-ideal behaviour in the CNT channel. The non-ballistic transport in CNTs is likely to attract more research attention in the near future. Elastic scattering mechanism in the CNT channel region conducts a reduced potential drop in the region. Channel resistance due to the elastic scattering increases which effects the drain current. Also change in band gap due to the strain effect on CNT and tunnel current causes the non-ballistic conditions over the CNTFET. In this paper, only the combined effects of these non-ideal approaches are considered. Also the effects of varying temperature are investigated in terms of on-state current, leakage off current,  $I_{ON}/I_{OFF}$  current ratio, quantum capacitance, insulator capacitance and drain-induced barrier lowering (DIBL). All

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these effects are analysed with different temperatures considering various high dielectric materials under non-ballistic regime.

## 2. Mathematical Model

This is a simple, analytical model that can be used to investigate the I-V characteristics of CNFET. The original model used MOSFET-like structure in order to investigate ballistic transport in CNFET since this structure has proved experimentally that it could achieve near ballistic transport [9]. At any specified drain/gate voltage, the drain current is calculated based on the total charge that occupied first subband in the nanotube. The process is repeated for all drain/gate voltage in the specified range before all the drain current values are plotted within a single graph.

This model has also been used for non-ballistic purpose. Moreover, different parametric simulation approach was also used [10]. A non-equilibrium mobile charge is induced in the nanotube due to an electric field between the drain and the source of a CNT transistor.

This mobile charge can be defined as

$$\Delta Q = q(N_s + N_D - N_0) \quad (1)$$

where  $N_s$  is the density of positive velocity states filled by

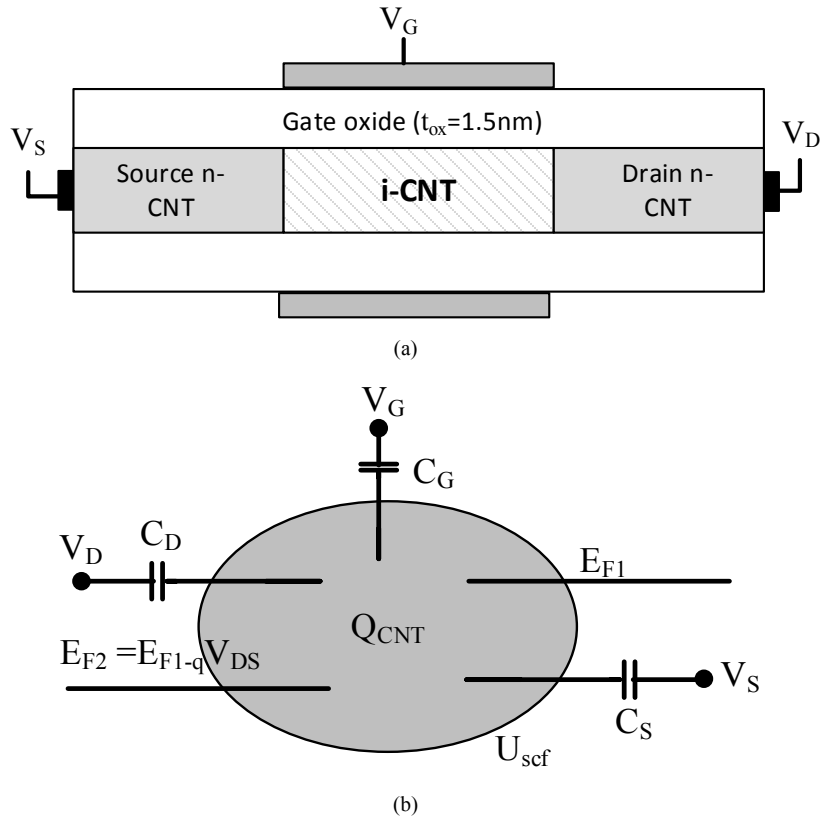
the source,  $N_D$  is the density of negative velocity states filled by the drain and  $N_0$  is the equilibrium electron density.

Elastic scattering has an impact on the channel length of the CNTFET and also in the mean free path (MFP). For this reason, the channel resistance is affected which introduced a modified drain voltage ( $V_{DS}$ ) due to elastic scattering. Therefore, the FET operates on a modified lower voltage, [10]

$$V_{Deff} = \frac{L}{L + \left(\frac{d}{d_0}\right)\lambda_{eff}} V_{DS} \quad (2)$$

Here,  $L$  is the channel length,  $d$  is the diameter,  $d_0$  is the reference diameter with a value of 1.5 nm.  $\lambda_{eff}$  denotes the elastic scattering MFP, the value of which is taken to be about 200 nm [10]. The transport properties of a CNT is also dependent on physical strain. When subjected to strain, the bandgap of CNT is changed and the effective bandgap is different from the actual bandgap. The new bandgap can be calculated using the following equation

$$E_{geff} = \frac{2a_{cc}V_{cc}}{d} + \frac{dE_{gstain}}{d\chi} \quad (3)$$



**Figure 1.** (a) Cross sectional view of the devices. (b). 2D Capacitor model for ballistic transistors. Top barrier potential controlled by capacitive effect of gate, source and drain potential [7]

Here,  $a_{cc}$ ,  $V_{cc}$  are the carbon  $\pi - \pi$  nearest-neighbor bond length and energy of the tight bonding model respectively and  $E_{geff}$  is the tuned bandgap in equation (3).

$dE_{gstain}$  is the shift of the bandgap because of strain and  $\chi$  is the distortion factor because of strain with a value of 0.1 [11].

Diameter of the nano tube depends upon the chiral indices and chiral angle. Diameter can be defined as

$$d = \frac{a}{\pi(\sqrt{n^2 + mn + m^2})} \text{ with } \varphi = \tan^{-1}\left(\frac{\sqrt{am}}{m + 2n}\right)$$

Here  $a$  is the atomic radius with a value  $2.49\text{\AA}$ ,  $n$  and  $m$  are chiral indices,  $\varphi$  is the chiral angle for a  $(n, m)$  CNT. The rate of change of the bandgap can be calculated using the following formula [11]

$$\frac{dE_{gstain}}{d\chi} = 3\sigma(1 + r_0)\text{sign}(2p + 1)\cos(3\varphi) \quad (4)$$

In equation (4),  $\sigma$  is the overlap integral of the tight-binding C-C model and it has a value of 2.7.  $r_0$  is the Poisson's ratio and for this research,  $r_0 = 0.2$ .  $p$  can be obtained using  $n - m = 3l - p$ .

The effect of tunnelling is calculated using a two-step method. In this way, at first, a parameter called tunnelling probability ( $T_t$ ) is introduced. When  $m^*$  is the effective mass,  $q$  is the charge of the electron,  $\hbar$  is the reduced Planck's constant and  $T_t$  is given by [11]

$$T_t \approx \frac{\pi^2}{9} e^{-\left(\pi\sqrt{m^*E_g^3}/\sqrt{8q\hbar F}\right)} \quad (5)$$

The entity  $F$  in equation (5) is termed as the tunnel control parameter. This parameter ultimately sets off tunnelling under a high electric field. The value of  $F$  has been extracted from figure 5 of [11] and have been found to be in the range of  $10^{36}$ . For simplification purposes, this work uses an average constant value of  $9.798 \times 10^{36}$  for  $F$  rather than using

it as a variable. The tunnelling current can be computed using

$$I_t = \frac{4qkT}{h} T_t \left[ \ln\left(1 + e^{(qV_{DSeff} - E_{geff}/2 - E_F)/K_B T}\right) - \ln\left(1 + e^{(qV_{DSeff} - E_F)/K_B T}\right) \right] \quad (6)$$

Here,  $E_F$  is the Fermi level and  $K_B$  is the Boltzmann constant in the equations.

Now to compute equation (1), densities are determined by the Fermi-Dirac probability distribution as follows [7]

$$N_s = \frac{1}{2} \int_{-\infty}^{\infty} D(E) f(E - E_{F_1} - qU_{scf}) dE \quad (7)$$

$$N_D = \frac{1}{2} \int_{-\infty}^{\infty} D(E) f(E - E_{F_2} - qU_{scf} - qV_{Deff}) dE \quad (8)$$

$$N_0 = \int_{-\infty}^{\infty} D(E) f(E - E_F) dE \quad (9)$$

Here  $E_{F_1}$  ( $E_{F_2}$ ) is the source (drain) Fermi level,  $f(E)$  is the probability that a state with energy  $E$  is occupied (Fermi-Dirac probability),  $D(E)$  is the nanotube density of states (DOS) at top of the barrier and  $U_{scf}$  is the self-consistent potential at the top of the barrier. For simplicity, assume source Fermi level as the reference, thus  $E_{F_1} = 0$  and  $E_{F_1} = -qV_{DS}$  where  $q$  is electronic charge.

The complete solution is found by adding the two contribution  $U_{scf} = U_L + U_P$  where,

$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S)$  Here  $\alpha_g$  and  $\alpha_d$  are gate and drain control parameters respectively. According to the ballistic CNT ballistic transport theory, the drain current caused by the transport of the non-equilibrium charge across the nanotube can be calculated using the Fermi-Dirac statistics as follows: [11]

$$I_{D1} = \frac{2qKT}{\pi\hbar} \left[ f_0\left(\frac{E_{F_1} - qU_{scf}}{KT}\right) - f_0\left(\frac{E_{F_2} - qU_{scf} - qV_{Deff}}{KT}\right) \right] \quad (10)$$

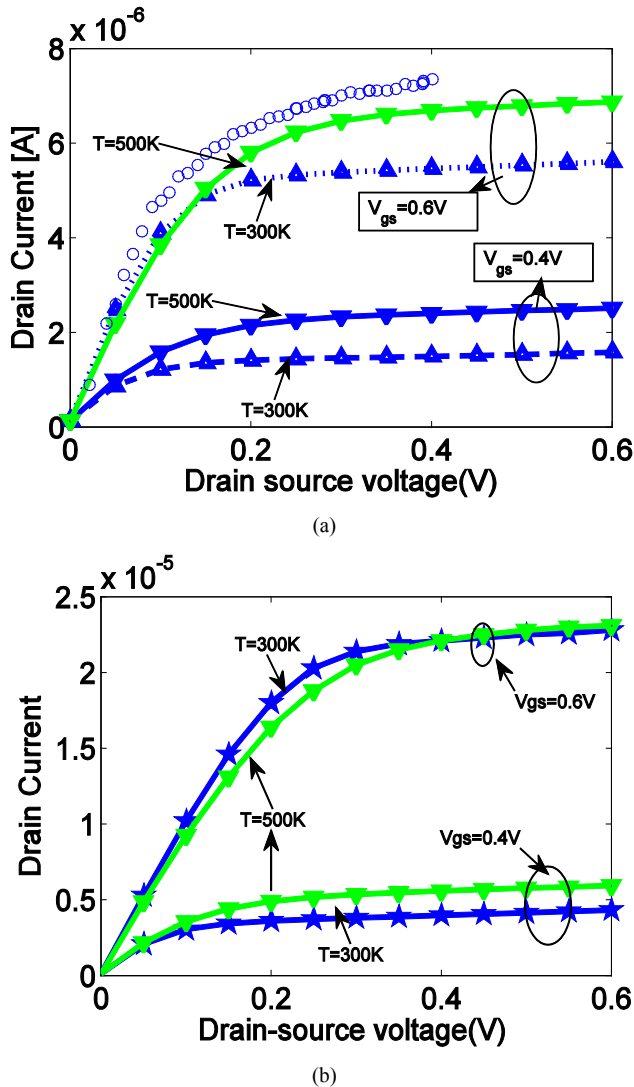
where  $f_0$  represents the Fermi-Dirac integral of order 0,  $T$  is the temperature and  $\hbar$  is the reduced Planck's constant. Here degeneracy factor is 2.

Finally, considering the non-ballistic effects, the total current would be the summation of the modified ballistic drain current and the tunnelling current. So the equation of the total current would be

$$I_D = \frac{4qK_B T}{h} T_t \left[ \ln\left(1 + \exp(E_{F_1} - U_{scf})\right) - \ln\left(1 + \exp(E_{F_1} - U_{scf})\right) + \left( \ln\left(1 + e^{(qV_{DSeff} - E_{geff}/2 - E_F)/K_B T}\right) - \ln\left(1 + e^{(qV_{DSeff} - E_F)/K_B T}\right) \right) \right] \quad (11)$$

### 3. Results and Discussions

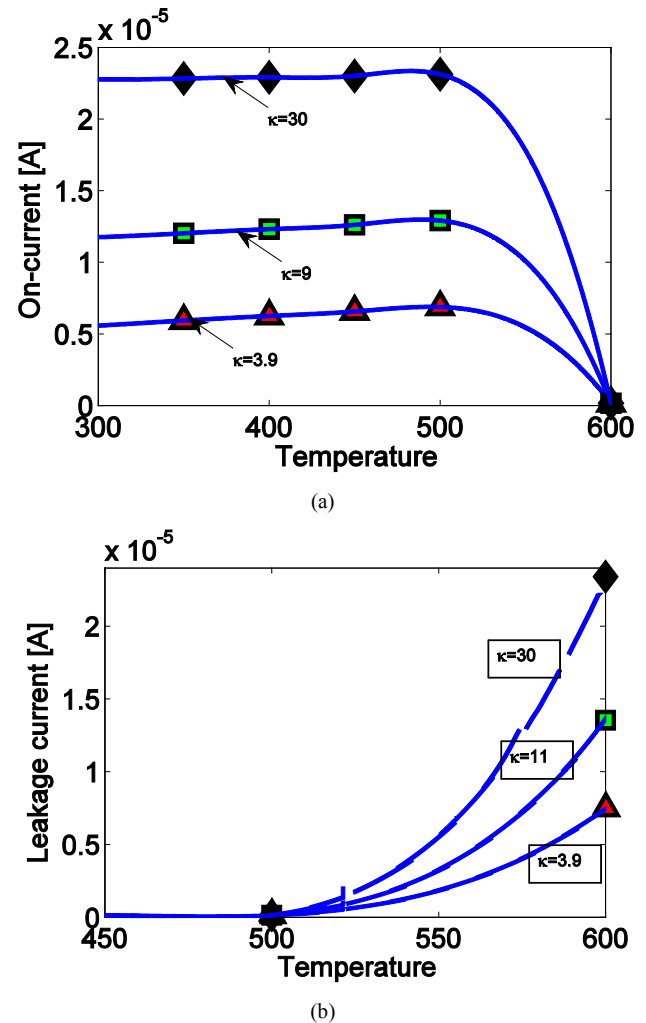
This CNTFET configuration considers a (13,0) zigzag CNT with a bandgap  $\sim 0.83\text{eV}$  and a diameter  $\sim 1.02\text{nm}$ . The oxide thickness is taken as  $1.5\text{nm}$  which separates the coaxial gate from the intrinsic part of the nanotube. The simulation is done with a gate and drain control parameters of  $0.88$  and  $0.035$ . In addition, the source Fermi level was chosen to be  $-0.32\text{eV}$ . To investigate the influence of the temperature on the attributes of CNTFET, the temperature has been varied from  $300\text{K}$  to  $500\text{K}$  under different dielectric constant values. Different dielectric constants has been taken for this simulation. To plot the I-V curves, the gate and drain voltages were both been varied from  $0$  to  $0.6\text{V}$ .



**Figure 2.** Comparison of the output characteristics ( $I_D$ - $V_{DS}$ ) of the CNTFET in  $300\text{K}$  and  $500\text{K}$  with different gate biases. (a) with dielectric constant  $3.9$  with experimental data (circlet lines) (b) with dielectric constant  $30$

Figure 2 (a) and (b) illustrates the output characteristics of the predefined structures at the room temperature and extreme condition with different dielectric constants. It can be seen that some reported experimental characteristics were compared with the simulation results for  $d = 1.6\text{ nm}$ ,  $t_{ox} = 50$

$\text{nm}$ ,  $T = 300\text{K}$ , and  $E_f = -0.05\text{ eV}$ . The experimental data are extracted from fig 2 of ref [11]. There are some variations between experimental and simulated one as the parameters are different. It can be seen that, with increase in temperature, drain current is also increasing with a low gate source voltage. From figure 2(a) it is also evident lower temperature ( $300\text{K}$ ) has a higher drain current than  $500\text{K}$ . When the gate voltage is high this condition is valid at low drain voltages, despite of non-ballistic conditions. However, in saturation regime, the higher temperature drain current dominates the lower ones like ballistic region. Figure 2(b) shows comparison of the output characteristics ( $I_D$ - $V_{DS}$ ) of the CNTFET in  $300\text{K}$  and  $500\text{K}$  with different gate biases with dielectric constant value of  $30$ . The figure depicts that with higher dielectric constant, the drain current at saturation region and at  $V_{GS}=0.6\text{V}$ , becomes approximately equal despite of temperature variations. Also the magnitude of the drain current rises high with high dielectric constant value.

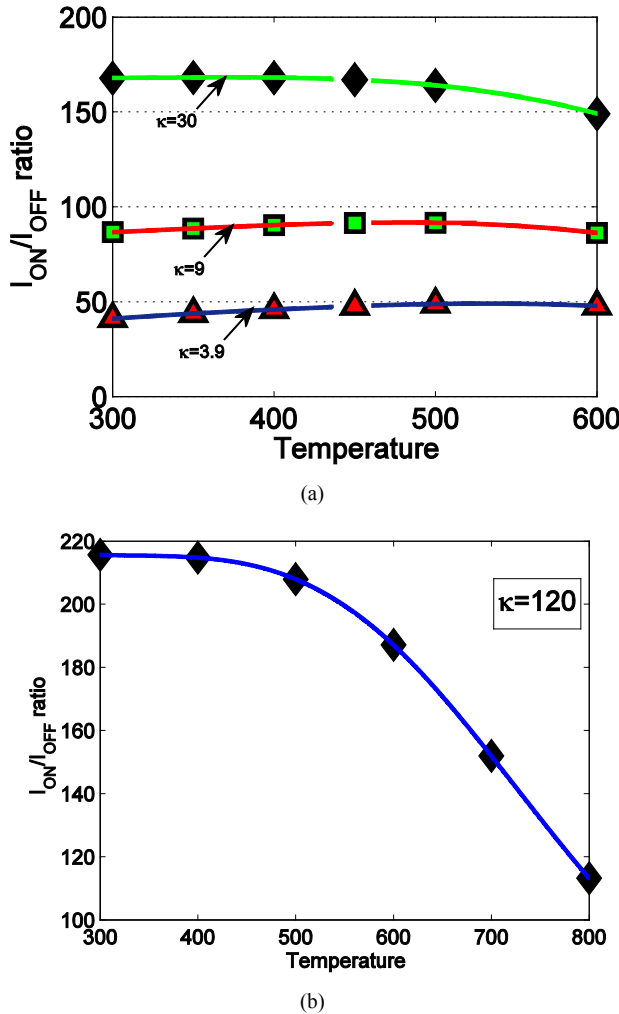


**Figure 3.** (a) On-state drain current versus Temperature at  $V_{GS}=0.6\text{V}$  and  $V_{DS}=0.6\text{V}$  with different dielectric constants. (b) Leakage current as a function of temperature at  $V_{GS}=0\text{V}$  and  $V_{DS}=0.6\text{V}$  with different dielectric constants

Figure 3 (a) shows on-current versus temperature curve with different dielectric constant at  $V_{GS}=0.6\text{V}$  and  $V_{DS}=0.6\text{V}$ .

The on-state current increases with the increase of temperature. The slope is almost constant. Also with higher value of dielectric constant, although the magnitude of the on-state current increases, the rate of increment of the on-state current for different  $\kappa$  values, remains same. This effect is clearly shown on the  $I_{ON}/I_{OFF}$  current ratio. However, with the increase of temperature beyond 500K on-state current decrease rapidly.

On the other hand, figure 3(b) shows the off-state current with different values of  $\kappa$ . In this case, gate voltage is kept zero and the drain voltage remains at 0.6V. The leakage current remains almost same for the lower temperature. After 500K, with a high  $\kappa$  value, the leakage current increases as the temperature increases. The rate of change in leakage current for high  $\kappa$  value is higher than low  $\kappa$  values with the increase in temperature beyond 500K. The current increases almost 20 times in 100K differences which is  $\sim 3$  times less than the ballistic regime with different condition [5]. Although the magnitude of the leakage current is less in non-ballistic conditions compared to ballistic one, the trend remains almost same.

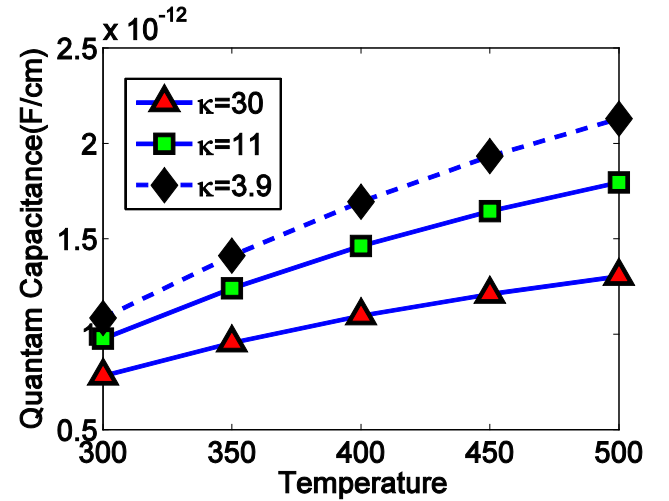


**Figure 4.**  $I_{ON}/I_{OFF}$  current ratio versus Temperature (a) for different dielectric constant (b) for a higher value ( $\kappa=120$ ) of dielectric constant

Figure 4 (a) and (b) shows the temperature effect on the

$I_{ON}/I_{OFF}$  current ratio with different  $\kappa$  values. Here the saturation current ( $I_{ON}$ ) is the drain current at  $V_{GS}=0.6V$  and  $V_{DS}=0.6V$  and the leakage current ( $I_{OFF}$ ) is the drain current at  $V_{GS}=0V$  and  $V_{DS}=0.6V$ . Figure 4 (a) reports the change in  $I_{ON}/I_{OFF}$  with different dielectric constant. Under different experimental setups mentioned in ref [15], it was reported that n-type CNT transistor fabricated with K-doping and grounded back gate, yields an  $I_{ON}/I_{OFF}$  current ratio of  $10^0$  to  $10^2$ . The effect of non-ballistic conditions are prominent on the  $I_{ON}/I_{OFF}$  current ratio as the range is less than 3 order magnitude than the ideal one. However, higher values of dielectric constants has a positive influence on the current ratio as it approaches towards the ideal ballistic current ratio range of  $10^5$ .

Figure 4(a) also depicts the change in current ratio under different range. For lower  $\kappa$  values from 300K to 450K, the rate remains almost same. However, figure 4(b) shows the impacts of the temperature on the current ratio with high dielectric constants. For a higher  $\kappa$  value ( $\sim 120$ ), the current ratio leads towards the ideal range despite of the non-ballistic effects in room temperature. It is clear that by increasing the temperature above 500K, the current ratio diminishes linearly for all range of  $\kappa$  values. Rate of increase in thermionic emission leakage on the top of the potential barrier makes the leakage current high. [13]. As a result, for high  $\kappa$  values, the current ratio decreases almost continuously by increasing temperature.



**Figure 5.** Quantum Capacitance vs Temperature for different dielectric constants

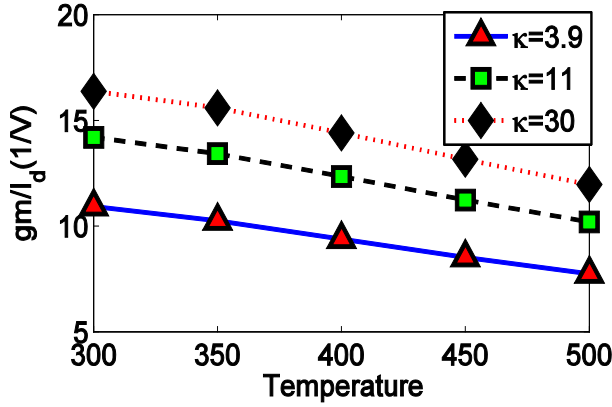
Quantum capacitance concept has an important impact on nano scale devices [15]. Quantum capacitance can be defined as

$$C_Q = \frac{\partial Q}{\partial V_a} \quad (12)$$

Here,  $Q$  is the charge density and  $V_a$  is local electrostatic potential. The limit of  $C_Q$  is vital in case of propagation delay parameter where total capacitance is

considered [15].

As shown in figure 5, the value of quantum capacitance increases as the temperature increases. Also with a higher value of  $\kappa$ , the value remains small which effects the performance of CNTFET devices in an adverse way. In this simulation gate voltage is taken as 0.3V.



**Figure 6.** Variation of  $gm/Id$  (1/V) ratio vs Temperature with different  $\kappa$  values

The variation of  $gm/Id$  ratio with respect to temperature for various dielectric materials of CNTFET as shown in Fig. 6. Here gate voltage is taken as 0.3V and drain voltage is 0.05V. As  $I_{ON}/I_{OFF}$  current ratio goes up with higher  $\kappa$  with lower temperature, ON-state current goes high. This increases the transconductance of the device. In order to achieve a relatively large transconductance the CNTFET must have higher value of  $\kappa$  at room temperature. The larger the transconductance, the greater the gain it will deliver. It has been observed that as temperature increases, the  $gm/Id$  ratio decreases due to the reason that the gate oxide capacitance is increased with high value of  $k$ .

Figure 7 shows the capacitance ratio versus Temperature for different dielectric constants. Here  $C_Q$  and  $C_{INS}$  defines as quantum capacitance and insulator capacitance respectively.

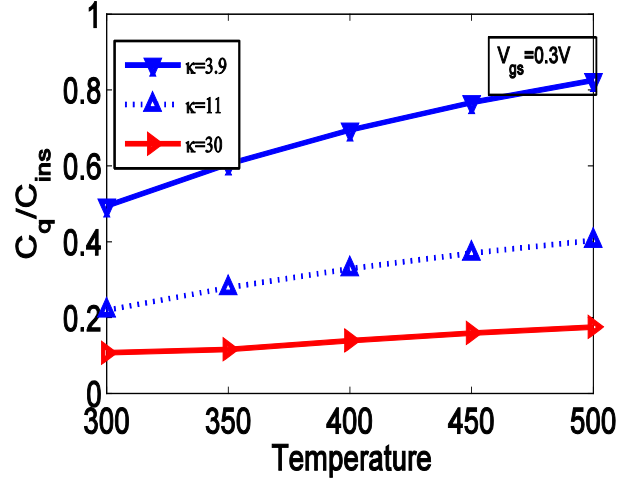
Insulator capacitance can be defined as [15]

$$C_{ins} = \frac{(2\pi\kappa\epsilon_0)}{\ln\left(\frac{2t_{ox}}{d}\right)} \quad (13)$$

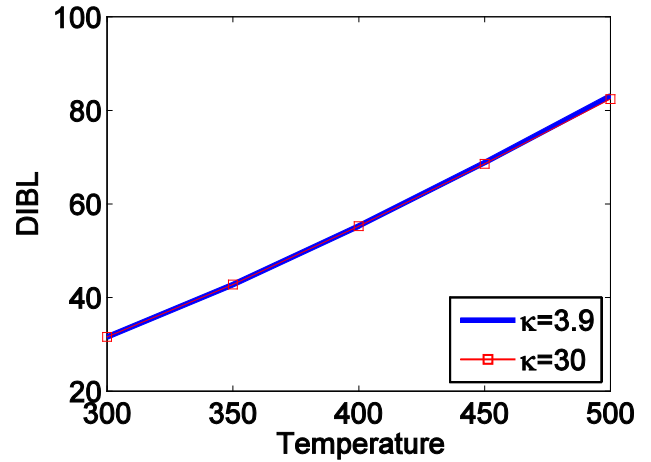
Here  $\epsilon_0$  is the permittivity of free space ( $F/cm^2$ ). The small value of the ratio indicates that in deep nanometer regime, quantum capacitance in CNTFET devices decreases. So an ambient temperature as well as optimised choice of dielectric constant value should be chosen for designing a devices. Also a higher quantum capacitance/insulator capacitance can be reached at a gate voltage of 0.3V with higher dielectric constant value. So lower gate voltage shows significant capacitive effect.

Figure 6 shows the drain induce barrier effect (DIBL) as a function of temperature. DIBL increases the leakage current with the capability of swinging the channel from off state to conduction state. As a result, it turns the device ON very

quickly and hence lowers down the threshold voltage. So the control of the gate voltage over the channel is reduced. Also with higher value of dielectric constants the DIBL remains almost unchanged. Due to all this reasons, the circuit should be designed with a reduced DIBL effect. The figure shows that by increasing the temperature the undesirable DIBL increases.



**Figure 7.** Capacitance ratio vs Temperature for different dielectric constants



**Figure 8.** Drain-induced barrier lowering (DIBL) as a function of temperature with different dielectric constant

## 4. Conclusions

In this paper the attributes of carbon nanotube field-effect transistors (CNTFETs) by varying the temperature with respect to different dielectric constants have been comprehensively investigated under non-ballistic condition. Under higher value of temperature and dielectric constants, current ratio decreases. Also drain current under different temperature with different dielectric constant changes with a less magnitude in non-ballistic condition comparing to the ballistic one. However higher  $\kappa$  value has little impact on the DIBL effect comparing to the temperature effect. So suitable  $\kappa$  with ambient temperature should be chosen for design.

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