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Design of Field-programmable Operational Transresistance Amplifier using Floating-gate MOSFETs

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Abstract We propose a comprehensive design procedure to design Field-programmable/Reconfigurable Analog Integrated CMOS circuits. Instead of repeatedly iterative simulation steps to achieve desired design specifications by fine tuning the W/L ratios of the FETs, we use first order classroom equations to achieve central value of desired specifications and then execute a customized fine tuning of specifications to the customers requirement with the help of Floating-gate Transistors FGMOS. To demonstrate the proposed design cycle, a modified high frequency/RF Operational Transresistance Amplifier (OTRA) CMOS circuit is designed where transresistance gain and input output low impedances are programmable, independently to desired values within a specific field range, using FGMOSs. In FGMOS the programmable charge at floating-gate using external voltages can results in threshold voltage field-programming, which in turn program the design (OTRA) specifications. With specific sizing and biasing condition, the transresistance can be programmed from 0.5kohm to 6kohm, input and output impedance from 600ohm to 10Kohm, while offset current can also be compensated independently using respective FGMOSs with 13-bit programming precision. However the final circuit, with four FGMOS occupies 75 µm × 64µm chip area. The design also consumes less power, total power consumption is about 3.96mW and show good thermal stability as output voltage variation with temperature is about 25 µV/ ℃.

Keywords Floating-gates, Field Programmable Analog Array, Operational Transresistance Amplifier, Specifications, Threshold Voltage

1. Introduction

The growing demand for mobile communications has led to high level of chip integration and directed research towards the field of high frequency applications. In the new designed circuit topologies for high frequency signal processing conventional methods based on voltage op-amp are no longer adequate as op-amp has a closed-loop gain dependent bandwidth, thus current-mode approach is preferred. Current mode circuits has potential advantages over their voltage counterparts, such as their inherently wide bandwidth, higher slew-rate, greater linearity, wider dynamic range, simple circuitry and low power consumption[1] and hence suitable for high frequency operations. In 1985 the popularity of current feedback op-amp amplifiers (CFOA) has increased considerably as they were found to be able to overcome the limitations arising from conventional operational amplifiers[2]. The term current-feedback is used because the error signal entering at the feedback node of the op-amp is in the form of a current and this gives to the amplifier a constant closed loop bandwidth capability[3]. Since the CFOA has a larger bandwidth and a higher slew-rate than the conventional op-amp, analog signal processing circuits built around the CFOA are expected to operate at higher frequencies than the op-amp based circuits[4].

An alternate current-mode circuit, operational transresistance amplifier (OTRA), is a three terminal analog building block shown symbolically in Figure 1(b) and defined using matrix, shown in Figure 1(b)[5]. It has similar transmission properties to the current-feedback op-amp, with an addition of two low-impedance inputs and one low-impedance output. OTRA, which is commercially available under the name of Norton amplifier (like Z10040A Norton noiseless feedback Amplifier[6]) have been attracted attention by its advantages in the current-mode circuit design. These commercial realizations do not provide a true virtual ground at the input terminals and they allow the input current to flow in one direction only. The former disadvantage limited the functionality of the OTRA whereas the latter forced to use external dc bias current leading complex and unattractive designs[7]. In order to remove these disadvantages of the OTRA, some topologies are proposed

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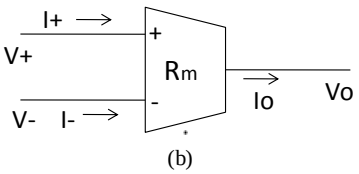
in the literature[8-10]. But these solutions are both complex structures and they do not operate properly at low power supplies, however in future design concept the main interest is designing circuitries with low power supplies. This demand leads designing a high performance CMOS differential OTRA for the current-mode analog systems design[11-14]. In CMOS OTRA design both the input and output terminals are characterized by low impedance. The input terminals are virtually grounded leading to circuits that are insensitive to stray capacitances[5]. Ideally the transresistance gain, Mr., approaches infinity, and applying external negative feedback will force the two input currents I+ and I−, to be equal (see Figure 1). This leads to growing interest for the design of OTRA-based analog signal processing circuits, such as instrumentation amplifiers MOSFET-C differentiator, integrators, continuous-time filters, immitance simulators, waveform generators, bistable multivibrators, oscillators[15-24]. A low-pass, band-pass, high-pass, and band-reject biquad filter is proposed using two OTRAs, three capacitors, and several resistors[19]. The phase shifter uses n-OTRA is tunable and blocks to give a total of n+1 oscillation[20]. A voltage-mode proportional-derivative using single OTRA, two resistors and a capacitor, having orthogonally tunable proportional and derivative constants[25] is proposed. Similarly a single OTRA with a capacitor and five resistors are used to propose a grounded negative inductance emulator with full independent control on both the inductance value and the condition[10]. These circuits require additional circuitry to introduce tuning ability within them. Thus programmable devices are required for accurate prototyping/on-chip tuning ability of the design. These circuits also experience limitation in applications like in highly integrated portable electronic devices, where less power consumption and small size hardware with higher integration is required. Moreover, there are various electronic systems where high precision tuning ability/programmability is required like for biologically inspired circuits such as bionic ear processor, learning circuits and related adaptive filters, neuromorphic and cellular computing circuits, etc. Instead of using additional circuitry we would like to modify the basic OTRA CMOS circuit[5] using Floating-gate Transistors (FGMOS) in place of conventional MOS, to introduce non-volatile, high precision on-chip programming in the OTRA design.

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_0 \end{bmatrix}$$

(a)



(b)

Figure 1. (a) I-V Describing matrix of OTRA (b) Schematic Diagram of OTRA

The circuit is designed using a comprehensive design procedure which allows post fabrication and independent tuning of critical specifications to desired values within a specific field range using analog voltages. Thus we propose a design procedure where instead of repeatedly iterative simulation steps to achieve very precise design specifications by fine tuning the W/L ratios of the FETs, we use first order classroom equations to achieve central value of desired specifications and then execute a customized fine tuning of specifications to the customers requirement. While maintaining small size and low power consumption, FGMOS are introduced in place of conventional MOS device hence conductivity of a MOS can be corrected by altering its threshold voltage (VT) by a field user[26, 27]. The OTRA circuit is analysed and derived in terms of design specifications whose derived equations show direct dependence on MOS thresholds. FGMOS offers continuous variation in threshold by storing the weights in a non-volatile analog memory with high accuracy[28, 29, and 30]. And the charge once stored at FG can be retained for more than 10 years. The proposed programmable OTRA design will not required extra hardware for storing, no digital code controlling circuitry however it will require interconnects to provide desired analog voltages to program floating gates of respective FGMOSs. In paper, parametric analysis of each OTRA design specification with respect to respective MOS is performed and hence, the circuit is modified with FGMOSs, which provide independent programming ability of design specification as well as circuit offsets, after fabrication. The total power dissipation and thermal stability of the modified design is also being catered in the paper. Such consistent approach to introduce programmability can be applied to various analog ICs (the idea of programmability using floating gate transistor is being published in conferences before[31, 32 and 33]).

2. Proposed Analog Design Cycle

Although vigorous development of consumer electronic products has been propelled by advancements in digital processing technology, the world is still analog. Sound, video and image are always represented in the form of analog signals. Analog designs tend to have higher integration density, consume less power and interface easily with the real world yet they are still less preferred option compared to their digital counterparts as analog implementation lacks accurate convertibility of design to prototype, stability of devices, long term storage of analog signals, field programmability and automated design. Analog design is more concerned with the physics of the semiconductor devices such as gain, matching, power dissipation, and resistance. However, fidelity of analog signal amplification and filtering is usually critical and as a result, analog IC design is critical. Thus there is a drive towards shorter design cycles for analog integrated circuits, which demand the development of high performance analog circuits that are reconfigurable and suitable for CAD methodologies[34].

Several manufactures have made programmable analog circuits; among these are Motorola, IPM Inc, Lattice and Anadigm. Several designs of Field Programmable Analog Arrays (FPAA) have been reported[35]-[38], but these are often aimed at a commercial market as an analog counterpart to Field Programmable Gate Arrays (FPGA) for rapid prototyping of analog circuits. Subsequently to introduce programmability in analog designs programmable device are also developed such as various methods are developed to modify electrical characteristics of MOS device which in turn introduce programming ability in MOS. It is performed either through openings in the passivation layer to define location of bonding pad or through ion implantation at exposed underlying polysilicon gate structure which create an implantation layer at the channel regions of selected MOS devices, and thereby permanently alter the threshold voltages of these MOS devices[39, 40]. However over the last decade there is a new technology based on floating gates have developed and floating gate circuit approaches have progressed from a few foundational academic results to stable circuits. Floating gate MOS are like conventional MOS with an additional gate in which by modifying the charge at the floating gate MOS characteristics (threshold) can be programmed on-chip after fabrication with real time, non-volatile, reconfigurable programming[41-43]. This programmable analog technology empowers analog signal processing approaches programmable precision analog low-power techniques[44].

Moreover as we move into more advanced CMOS process nodes, it has become apparent to the designers that although the fundamental RF/analog design principles remain unchanged, there have to be new techniques and architectures to fully harness the potential of CMOS scaling and to advance the state of the art. So inspired from floating gate MOS technology, we would like to propose a paradigm shift in analog circuit designing where instead of repeatedly iterative simulation steps to achieve very precise design specifications by fine tuning the W/L ratios of the FETs, we use first order classroom equations to achieve central value of desired specifications and then execute a customized fine tuning of specifications to the customers requirement. The proposed analog design cycle flowchart and algorithm is illustrated in Figure 2. As conventional Analog design cycle consists of basic five steps: system modelling, circuit simulation, layout, physical verification and post layout verification i.e. it is useful to first model the behaviour of those system to understand its stability condition and system response, then for targeted specifications some changes such as architectural change in circuit, resizing of transistors might be needed. This can be achieved by manual design, table-based calculation employing Excel or Matlab, circuit sizing by Genetic Algorithms or Particle-Swarm-Optimization or by circuit simulations like SPICE. However, troubleshooting of each step is very complicated. It is a loop linked back to the previous steps and possibly troubleshooting all the way back to step1. However our approach towards circuit design is different because with the help of post fabrication programmability feature in FGMOSs, desired specification values can be adjusted by a field user

Algorithm:

1. Analyse circuit with the help of block diagram to establish desired functionality.
2. Simulate the circuit to check its functionality with basic sizing and biasing conditions.
3. Design the equivalent small-signal model of the circuit.
4. Derive specifications in terms of threshold voltage of transistors.
5. Analyse sensitivity of each specification with respect to respective thresholds.
6. Simulate the circuit to check the sensitivity of each specification.
7. Layout creation and verification of the circuit with basic sizing and biasing conditions. Then after testing and extraction, fabricate the design.
8. Program the transistor's thresholds to adjust the desired specifications with huge accuracy

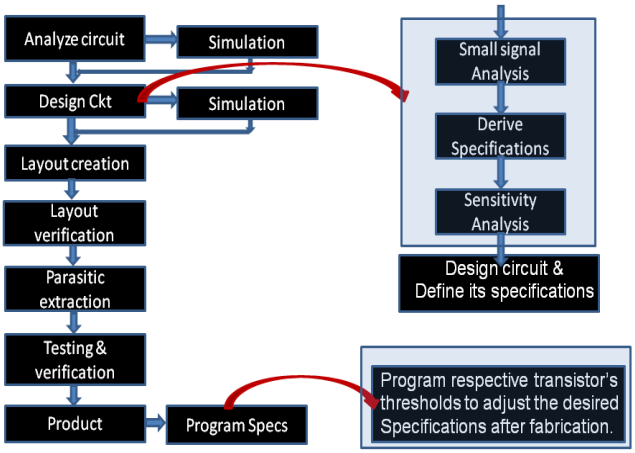


Figure 2. Flowchart of Proposed Analog IC Design Procedure

Hence the accurate reconfigurable prototype of the design can be developed after fabrication. An added advantage is that the designs are reconfigurable, i.e. for a new derivative of the design or the same design with new value of specifications can be developed using on-chip programming ability unlike conventional design flow where new design configuration need to follow the complete design cycle again. Therefore this design analogy saves design time and cost. The tradeoffs between accurate and optimize design which analog designer has to maintain throughout the design procedure does not remain the major issue while designing analog circuits now. As with the proposed design flow optimized design can be fabricated and final accurate prototype with fine on-chip tuning can be derived.

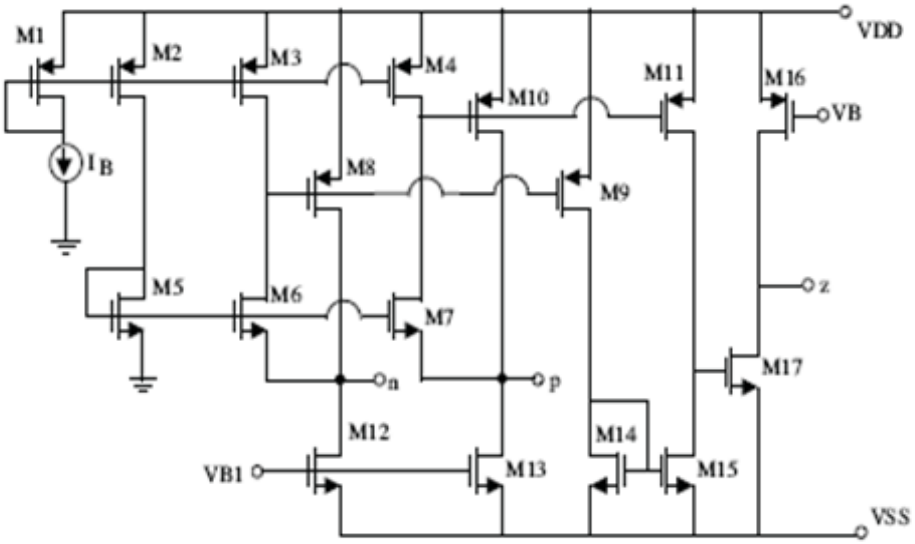
2.1. Design Objectives

Before designing or introducing programmability in OTRA CMOS circuit few design objectives need to be considered. Firstly the variation in the design specifications should be large and continuous. Indirect, non-volatile and high precision programming of FGMOS thresholds can

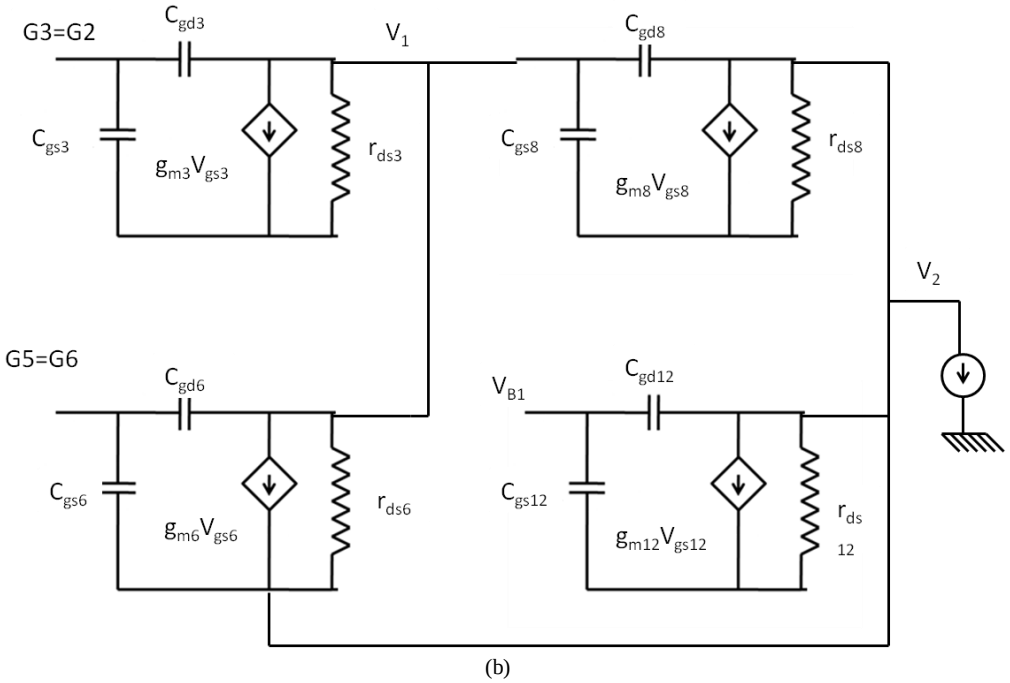
produce large range and continuous programming of specifications. However, large continuous variation in specifications is difficult and sometimes unstable. Second design objective is that the variation of each specification should be independent of the other i.e., each specification should be programmed either by one or more FGMOS but should not alter any other design specifications. However if specification programming are not independent then either through modifying the circuit or by compensating the affected specification value using different set of FGMOS, should be prepared. Thirdly, operating point of the circuit should not alter too much during programming, i.e. current density in each transistor should not change significantly or in other words offset current should not vary significantly.

3. Basic CMOS OTRA Design

The OTRA design is a three terminal device whose schematic diagram and its IV describing matrix is shown in Figure. 1. Both the input and output terminals are characterized by low impedance. Ideally the transresistance gain, R_m, approaches infinity and applying external negative feedback will force the two input currents, I+ and I-, to be equal. CMOS OTRA design[5] as shown in Figure 3(a) consists of cascaded connection of the modified differential current conveyor and a common source amplifier.



(a)



(b)

Figure 3. (a): Circuit diagram of CMOS OTRA[5] (b): High frequency small signal equivalent circuit loop of the OTRA

Assuming that each of the groups of the transistors are matched and all the transistors operate in the saturation region, the circuit operation can be explained as follows. The current mirrors formed by (M1-M4) forces equal currents (I_B) in the transistors M5, M6 and M7. This operation drives the gate to source voltages of M5, M6 and M7 to be equal and, consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs (M3 and M4), (M8 and M9), (M10 and M11) and (M14 and M15) provide the current differencing operation, whereas the common source amplifier (M17) achieves the high gain stage. The current biasing I_B is connected to the transistor M1 with common gate and thus biases the transistors M1 to M4. Transistors M3, M6, M8, M9 and M4, M7, M10, M11 form two loops which transmits the currents I+ (Ip) and I- (In) respectively. Hence the output voltage is produced with currents of M9 and M11 which biases the output stage transistors (M14 M15, M16 and M17) of OTRA design.

3.1. High-frequency Small signal Analysis

The OTRA design is operated at high frequency; accordingly high frequency small signal equivalent model is generated and design characteristics are derived. The circuit consists of two loops formed by M3, M6, M8, M9 and M4, M7, M10, M11 which propagates the input current In and Ip respectively. By applying KCL on high frequency small signal equivalent circuit as shown in Figure 3(b), expression for output voltage of OTRA at the output node is derived where current source is I+. The expression of output voltage is evaluated in terms of threshold voltages of MOSs when transconductance is replaced by their corresponding threshold voltages in expression. Hence output voltage can be programmed using threshold voltage of M16 and M17.

$$V_{out} = \frac{(sc_{gd\,16}+g_{m\,16})v_{b2}+(sc_{gd\,17}-g_{m\,17})v_{ds\,11}}{sc_{gd\,16}+sc_{gd\,17}+g_{ds\,16}+g_{ds\,17}} \quad (1)$$

Transresistance or design gain have been derived by dividing the output voltage with difference of input current and expressed as below which shows its dependence in terms of threshold voltages of MOSs M16 and M17.

$$R_m = \frac{(sc_{gd\,16}+g_{m\,16})v'_{b2}+(sc_{gd\,17}-g_{m\,17})v_{ds\,11}}{sc_{gd\,16}+sc_{gd\,17}+g_{ds\,16}+g_{ds\,17}} \quad (2)$$

$$v'_{b2} = \frac{v_{b2}}{I_+ - I_-} \qquad v'_{ds\,11} = \frac{v_{ds\,11}}{I_+ - I_-}$$

Expression of input impedance and output impedance of OTRA have been derived by dividing voltage to the current at the input and output respectively and expressed as:

$$Z_{in} = (sc_{gd\,3}+g_{m3})Cv_{gs\,3} + A(sc_{gd\,12}-g_{m12})v_{b1} - A + [(sc_{gd\,6}-g_{m6})C + A(sc_{gs\,6}+g_{m6})]v_{gs\,5} \quad (3)$$

$$Z_{out} = \frac{1+g_{m\,16}v_{gs\,16}-g_{m\,17}v_{gs\,17}}{sc_{gd\,16}+sc_{gd\,17}+g_{ds\,16}+g_{ds\,17}} \quad (4)$$

Input impedance of OTRA depends upon the threshold voltages of MOSs M3, M12, and M6, output impedance of OTRA is depends upon the threshold voltages of MOSs M16 and M17. Moreover offset voltage of OTRA is the output voltage when zero input currents are applied, which is expressed as equation22. It depends upon the threshold voltages of M17, M4, M11, M15, M10, M1, M9, M3, M8, I_b and hence it can be easily program with the threshold voltages of various MOSFETs.

$$V_{offset} = \frac{g_{m\,17}}{g_{ds\,16}+g_{ds\,17}}\left[\frac{g_{m\,4}^2 g_{m\,11}}{g_{m\,15}g_{m\,10}g_{m\,1}} + \frac{g_{m\,9}g_{m\,3}}{g_{m\,8}g_{m\,1}}\right] I_b \quad (5)$$

Thus design specifications are dependent on respective MOSs threshold voltages.

3.2. Characteristics of Basic OTRA design

The basic OTRA design has been simulated and its basic functionality with central value of specifications at specific biasing and sizing conditions of the circuit is estimated. Transistors aspect ratio is tabulated in Table1. The biasing current I_B = 5μA. The biasing voltages V_B = -1 V and V_{B1} =0.2 V. Thus at a specific sizing and biasing condition of the design, frequency response of transresistance gain magnitude and phase is represented in Figure 4(a) and (b). Figure 4(c) shows the frequency response of the input impendence and figure 4(d) depict temperature stability of the design. The variation in output voltage with changing temperature from -40 ℃ to 80 ℃ is about 25 μV/ ℃. The input differential current range is from -20μA to 20μA. The offset current equals 0.15μA. The input resistance equals 22.139 Ω. The output resistance equal to 12 KΩ. The DC open loop transresistance gain equals 4.054dBΩ (=1.67 KΩ). The gain bandwidth product equals 10.3 GHz Ω. The power dissipation of the circuit equals 9.34mW. The characteristics summary is tabulated in Table2. Hence the characteristic plots of the basic OTRA circuit shows its basic functionality as verified from papers[4-6].

Table 1. Transistor aspect ratio of the circuit in Figure 1(b)

M1-M4	17.5um(W)/0.7um(L)
M5-M7	35um(W)/0.7um(L)
M8-M11	17.5um(W)/0.7um(L)
M12-M15	7um(W)/ 0.7um(L)
M16	4.2um(W)/0.7um(L)
M17	17.5um(W)/0.7um(L)

Table 2. Main Characteristics of OTRA design at bias current, I_b =5 μA and biasing voltages= ±2.5v

Design parameters	Value
DC open loop transresistance	1.67Kohm (4.054dBohm)
Gain bandwidth product	39.8GHzohm
Input resistance	22.139ohm
Output resistance	12Kohm
Input current dynamic range	-20uA to 20uA
Offset current	0.15uA
Power dissipation	3.96mW

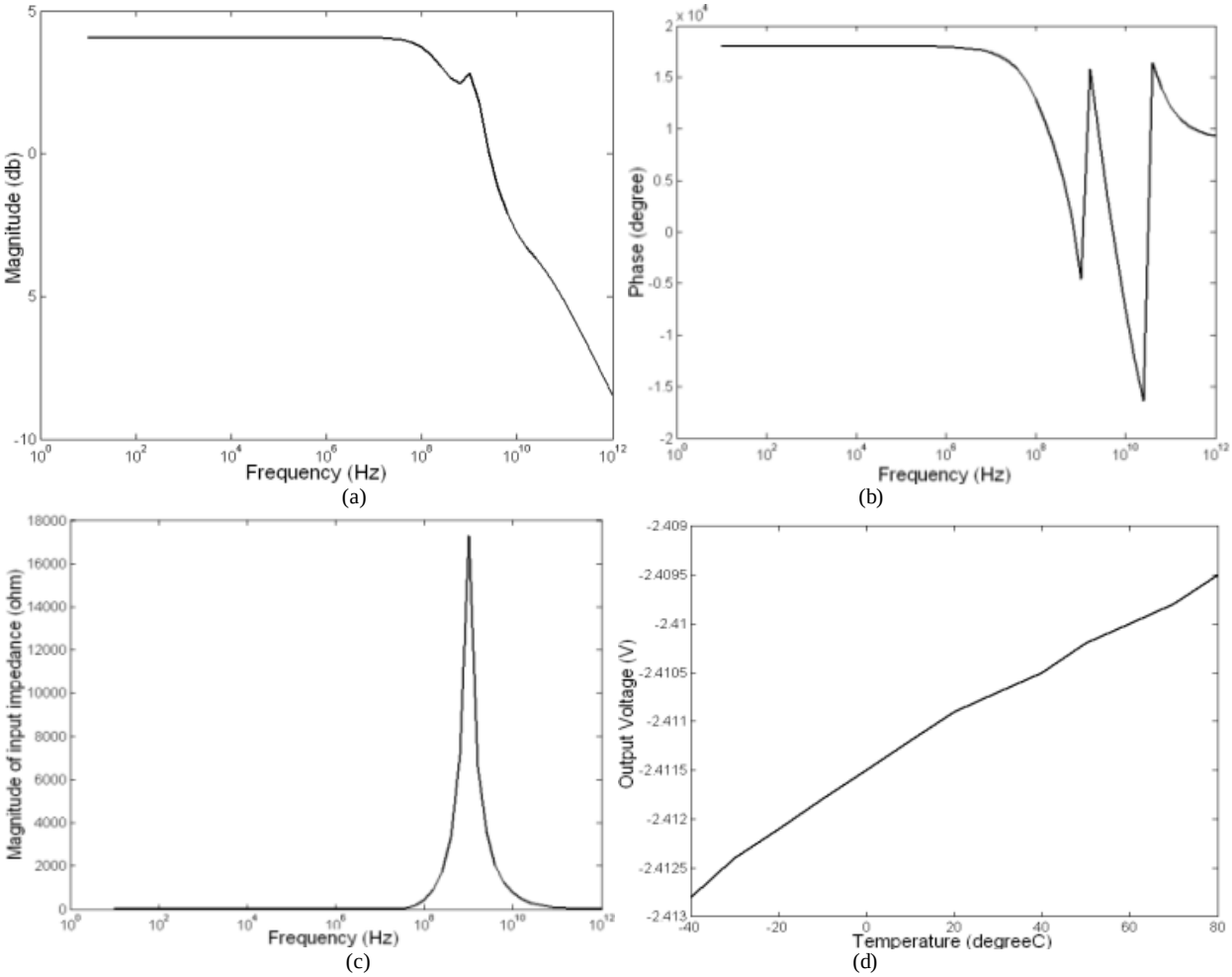


Figure 4. Frequency Response of (a) Transresistance magnitude (b) Transresistance phase I_p and I_n (c) Input impedance Z_{in} at port X of OTRA (d) Variation in Output voltage with changing temperature from -40 ℃ to 80 ℃

4. Design of Programmable OTRA

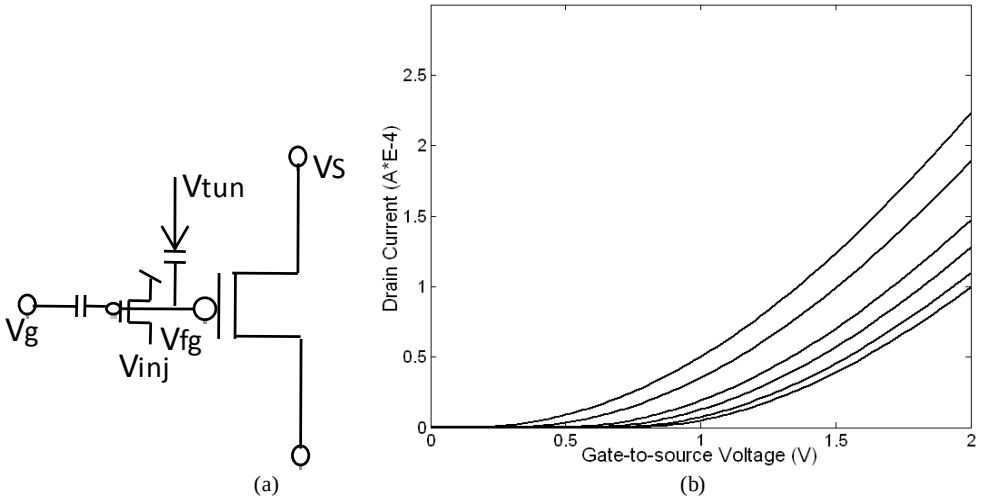
It is observed from simulation results of basic OTRA circuit that the OTRA circuit is justifying its basic characteristics. Now to introduce programmability in this basic OTRA circuit MOSFETs are replaced by floating gate MOSFETs. Floating-gate MOSFETs are conventional MOSFETs wherein memory is stored in the form of charge trapped on floating-gate, affecting its threshold voltage. Two antagonistic quantum mechanical transfer processes, viz. hot e- injection and Fowler Nordheim tunnelling, alter the trapped charge on a floating gate. As these processes can occur during normal operation (indirect programmable using hot e injection and Fowler Nordheim tunnelling simulation model[31, 32]), it leads additional attributes to the FGMOS transistors such as non volatile analog memory storage on floating-gate, locally computed bidirectional memory updates and memory modification during normal transistor operation. It is represented by symbol showing injection and tunnelling nodes, attached at the common floating gate in Figure 5(a).

Tunnelling

Charge is added to the floating gate by removing electron from it by means of Fowler-Nordheim tunnelling across oxide capacitor. This shifts the curve (Figure 5(b)) to the right or in other words threshold voltage of the transistor increases.

Injection

Charge is removed from the floating-gate by adding electron on it by impact-ionized hot electron injection from the channel to the floating gate across the thin gate oxide. This shifts the curve (Figure 5(b)) to the left or in other words threshold voltage of the transistor decreases.



(a) (b)

Figure 5. (a): Pictorial representation of a normal MOS with indirectly programmable floating gate using injection and tunnelling (b) Output Characteristics of a FGMOSFET

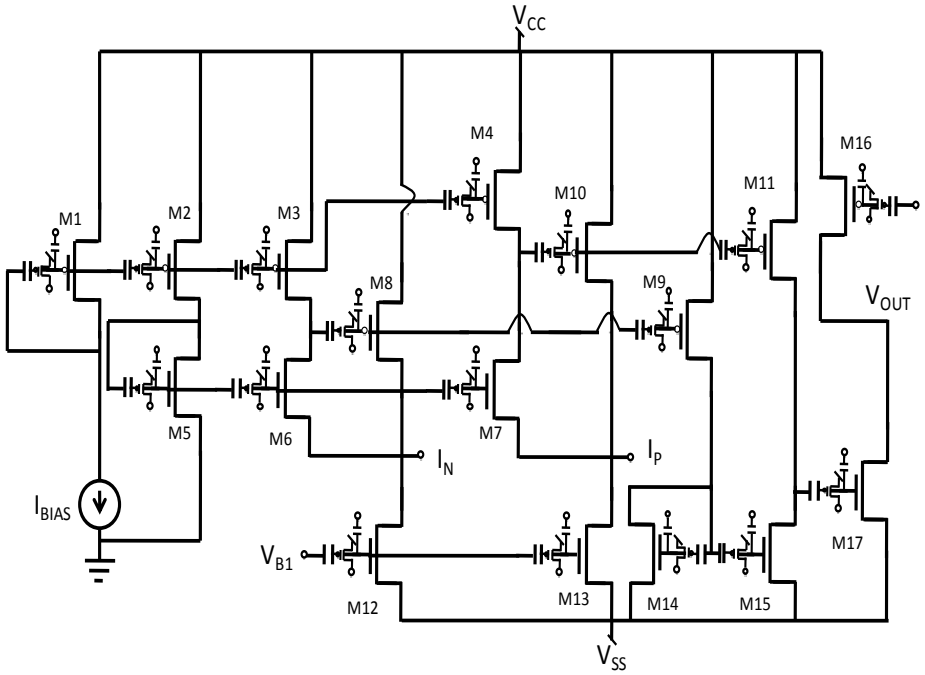


Figure 6. Circuit Diagram of proposed modified OTRA design whose specifications are programmable by field user to any desired value

Hence the modified OTRA circuit consists of floating gate MOSFETs, introduces programming ability of its design specifications and the circuit is represented in Figure 6. Design characteristics defined in last section can be expressed in terms of threshold voltages, by replacing transconductance of the respective transistors with their threshold voltages. Therefore basic characteristics of the design can be adjusted to desired value after fabrication using transistors with programmable threshold. Design steps are developed with which all design characteristics can be adjusted. Hence it save several simulation steps as accurate prototype of OTRA circuit can be developed using only first cut equations, as well as, it makes the circuit reconfigurable. With modified OTRA circuit, all design characteristics can be programmed independently with only one/two programmable thresholds. Equations expressing sensitivity of each specification with respect to respective FGMOSs have been derived and verified using simulation results.

4.1. Sensitivity Analysis of Design Specifications

Output Voltage: - Sensitivity of output voltage V_{out} has been evaluated using equation (1) which shows dependence on threshold of FGMOSs M16 and M17. Thus the sensitivity of V_{out} with respect to FGMOSFET M16 is calculated using partial differentiation of V_{out} w.r.t V_{t16} considering rest thresholds constant, is given by:

$$S_{v_{t16}}^{V_{out}} = \frac{-k_{16} v_{b2} v_{t16}}{(sc_{gd16} + g_{m16}) v_{b2} + (sc_{gd17} - g_{m17}) v_{ds11}} \quad (6)$$

Similarly sensitivity of output voltage with respect to the threshold voltage of M17, Vt17 is:

$$S_{v_{t17}}^{V_{out}} = \frac{k_{17} v_{ds11} v_{t17}}{(sc_{gd16}+g_{m16})v_{b2}+(sc_{gd17}-g_{m17})v_{ds11}} \quad (7)$$

Transresistance: - Sensitivity of output voltage Rm has been evaluated using equation (2) which shows dependence on threshold of FGMOSs M16 and M17. Thus the sensitivity of Rm with respect to FGMOS M16 is calculated using partial differentiation of Rm w.r.t Vt16 considering rest thresholds constant, is given by:

$$S_{v_{t16}}^{R_m} = \frac{-k_{16} v_{b2}' v_{t16}}{(sc_{gd16}+g_{m16})v_{b2}'+(sc_{gd17}-g_{m17})v_{ds11}} \quad (8)$$

Similarly sensitivity of Transresistance w.r.t to the threshold voltage of FGMOS M17, Vt17 is expressed as:

$$S_{v_{t17}}^{R_m} = \frac{k_{17} v_{ds11}' v_{t17}}{(sc_{gd16}+g_{m16})v_{b2}+(sc_{gd17}-g_{m17})v_{ds11}'} \quad (9)$$

Input impedance: - Similarly sensitivity of input resistance Zin has been evaluated using equation (3) which shows dependence on threshold of FGMOSs M3, M6 and M12. Thus the sensitivity of Zin with respect to FGMOS M3 is calculated using partial differentiation of Zin w.r.t Vt3 considering rest thresholds constant, is given by:

$$S_{v_{t3}}^{Z_{in}} = \frac{-k_3 v_{gs3} v_{t3} C}{Z_{in}} \quad (10)$$

Similarly sensitivity of Transresistance w.r.t to the threshold voltage of FGMOS M6, Vt6 is expressed as:

$$S_{v_{t6}}^{Z_{in}} = \frac{[k_6 C - k_6 A] v_{gs5} v_{t6}}{Z_{in}} \quad (11)$$

And sensitivity of Transresistance w.r.t to the threshold voltage of FGMOS M12, Vt12 is expressed as:

$$S_{v_{t12}}^{Z_{in}} = \frac{k_{12} v_{b1} v_{t12} A}{Z_{in}} \quad (12)$$

Output Impedance: - Sensitivity of output impedance Zout of OTRA expressed by equation (4) depends on threshold voltages FGMOSs M16 and M17. Thus sensitivity of Zout with respect to Vt16 is given by:

$$S_{v_{t16}}^{Z_{out}} = \frac{-k_{16} v_{gs16} v_{t16}}{1+g_{m16} v_{gs16} - g_{m17} v_{gs17}} \quad (13)$$

Sensitivity of output impedance Zout w.r.t to the threshold voltage of FGMOSFETM17 is expressed as:

$$S_{v_{t17}}^{Z_{out}} = \frac{k_{17} v_{gs17} v_{t17}}{1+g_{m16} v_{gs16} - g_{m17} v_{gs17}} \quad (14)$$

Offset Voltage: - However sensitivity of offset voltage of OTRA is calculated with respect to respective FGMOSs M17, M11 and M4 is given by:

$$S_{v_{t17}}^{V_{offset}} = \frac{-k_{17} v_{t17}}{g_{m17}} \quad (15)$$

$$S_{v_{t11}}^{V_{offset}} = \frac{-k_{11} v_{t11} g_{m4}^2 g_{m8} g_{m1}}{(g_{m4}^2 g_{m11} g_{m8} g_{m1}+g_{m9} g_{m3} g_{m15} g_{m10} g_{m1})} \quad (16)$$

$$S_{v_{t4}}^{V_{offset}} = \frac{-2k_4 v_{t4} g_{m4} g_{m11} g_{m8} g_{m1}}{(g_{m4}^2 g_{m11} g_{m8} g_{m1}+g_{m9} g_{m3} g_{m15} g_{m10} g_{m1})} \quad (17)$$

The sensitivity expressions have been verified using simulation results illustrated in next section and shown in Figure 7. Offset current can be corrected using above mentioned floating gate transistors. However the dominant FGMOS to program respective specification is identified. Simulation results illustrating such programming or sensitivity of respective characteristics while considering each transistor individually will be explained by plots in Figure 7 and programming steps along with programming range are tabulated in Table3.

4.2. Simulation Results Demonstrating Programming Steps to Program Circuit Specifications

The circuit diagram of Figure 4 representing modified OTRA design is simulated using BSIM3 level 49 MOSFET models using T-Spice 0.35µm CMOS process and the final circuit with essential number of FGMOS is verified using Cadence analog design tool, Virtuoso. Figure 7 (a)-(d) represent programmable transresistance gain magnitude, phase and input output resistance with respect to threshold of floating gate transistor M17, Vt17. From the plots it is verified that the transresistance magnitude can be programmed independently using threshold voltage of FGMOS M17, Vt17 as rest all specifications input resistance, output resistance even transresistance phase does not vary with Vt17. At particular sizing and biasing condition of the proposed OTRA circuit, the range of transresistance magnitude programming in decibels is from 2 dB to 8dB (= 0.5kohm to 6kohm) where rest all specifications remain constant. Similar variations of each specification with the respect to respective transistor have been performed and dominant FGMOS is identified. Figure 8(a) illustrates programming of input impedance with respect to FGMOS M6 threshold, Vt6. However while programming Vt6, changes occur in the value of transresistance magnitude. In addition to it, Figure 8(b) illustrates programming of output impedance with respect to FGMOS M14 threshold, Vt14. However while programming Vt14, changes occur in the value of transresistance magnitude. Therefore it is observed that each specification shows dependency on more than one FGMOS's threshold. So with some design modification as well as with iterative simulations each specification can be estimated to be programmed using only one FGMOS threshold, compensating change in rest all other specifications. Thus with iterative simulations and parametric analysis of each specifications, programming steps used to program design specification is tabulated in Table 3.

Figure 9 represent parametric analysis results of specifications with respect to respective threshold model parameter, threshold voltage, Vtx. The sensitivity analysis of all specifications w.r.t Vt17 is shown in Figure 9(a). Hence transresistance magnitude Rm can be programmed independently with Vt17, where no change in input, output impedance Zin and Zout and in offset voltage. Figure 9(b) represents that output impedance Zout dominantly vary with threshold of FGMOS M14, Vt14 where transresistance and offset voltage varies significantly, however, input resistance remain constant. Hence transresistance magnitude need to be compensated using FGMOS M17. Similarly sensitivity analysis of all specifications with respect to FGMOS M6 is illustrated in Figure 9(c). It shows that the input impedance Zin varies with threshold voltage of FGMOS M6 where transresistance also varies with M6 however output impedance remains constant. Hence to program input impedance with Vt6, transresistance need to be compensated using FGMOS M17 (Rm is sensitive to Vt17 as shown in

Figure 9(a)).

Therefore, the final modified circuit consists of four FGMOS which can program transresistance, input impedance, output impedance and offset voltage to any desired value within the defined range with very high precision.(about 13 bit programming resolution is observed and the same programming precision is claimed in paper[33]). Thus the final circuit consists of four FGMOSs and its circuit diagram and layout are shown in Figure 10(a) and (b). In addition to it, the programming steps which demonstrate the range and method to program circuit specifications is tabulated in Table3. The final OTRA design with help of four indirectly non-volatile field-programmable FGMOS, can program its design specifications along with offset output voltage with high accuracy, as illustrated in next section.

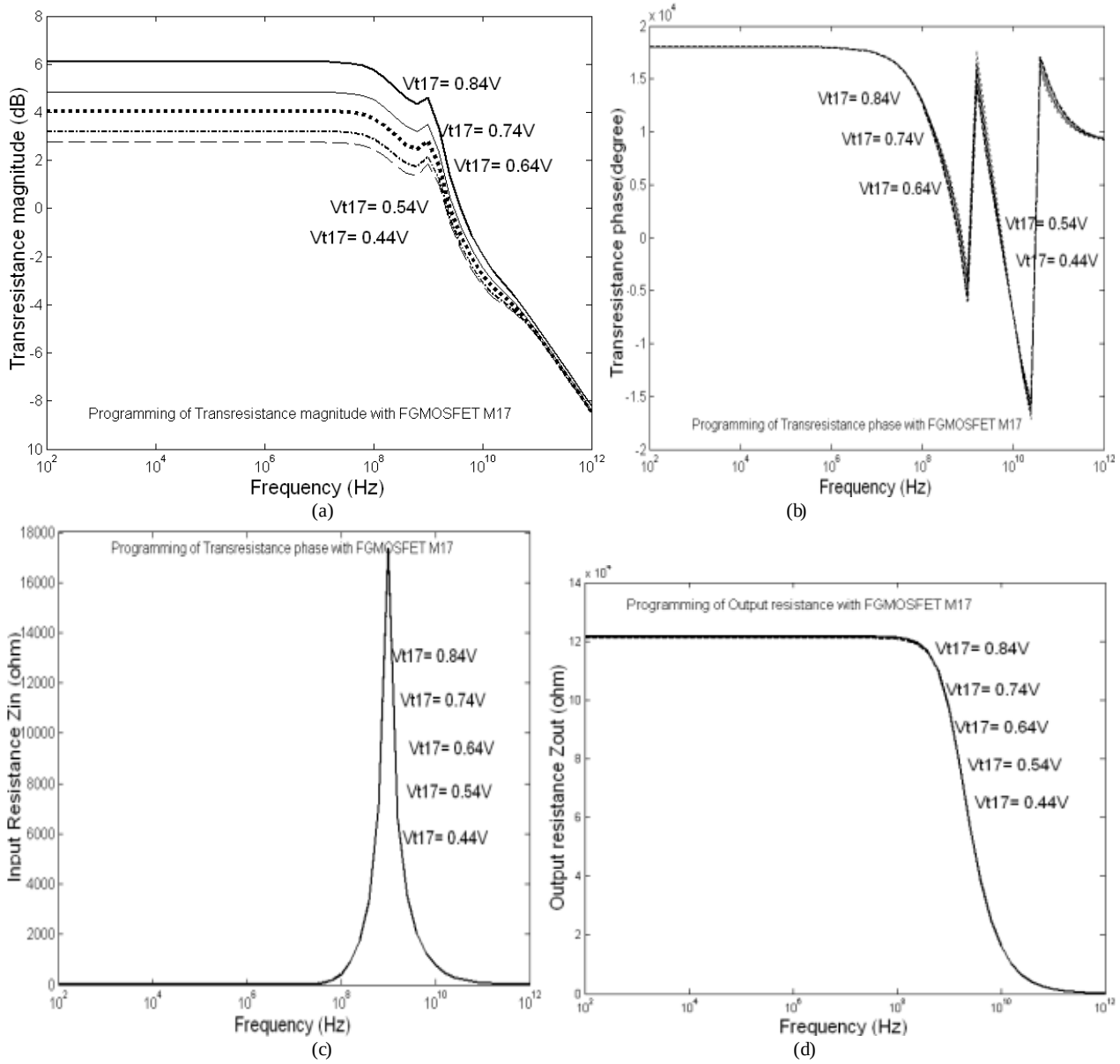


Figure 7. (a) Variation of Transresistance magnitude in dB with programmable thresholds of FGMOS M17 Vt17 (b) Variation of Transresistance phase in degree with programmable thresholds of FGMOS M17 Vt17 (c) Variation of input impedance Zin (ohm) with programmable threshold of FGMOS M17 Vt17 (d) Variation of output impedance Zout (ohm) with programmable threshold of FGMOS M17 Vt17

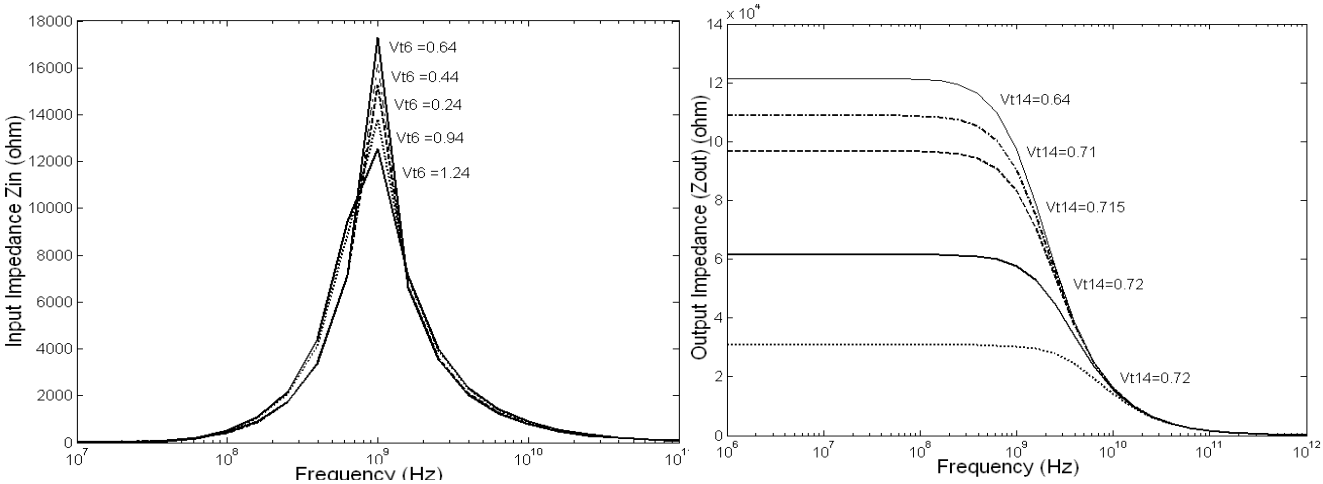


Figure 8. (a) Variation of input impedance Z_{in} (ohm) with programmable threshold of FGMOS M6 V_{t6} (b) Variation of input impedance Z_{out} with programmable threshold of FGMOS M14 V_{t14}

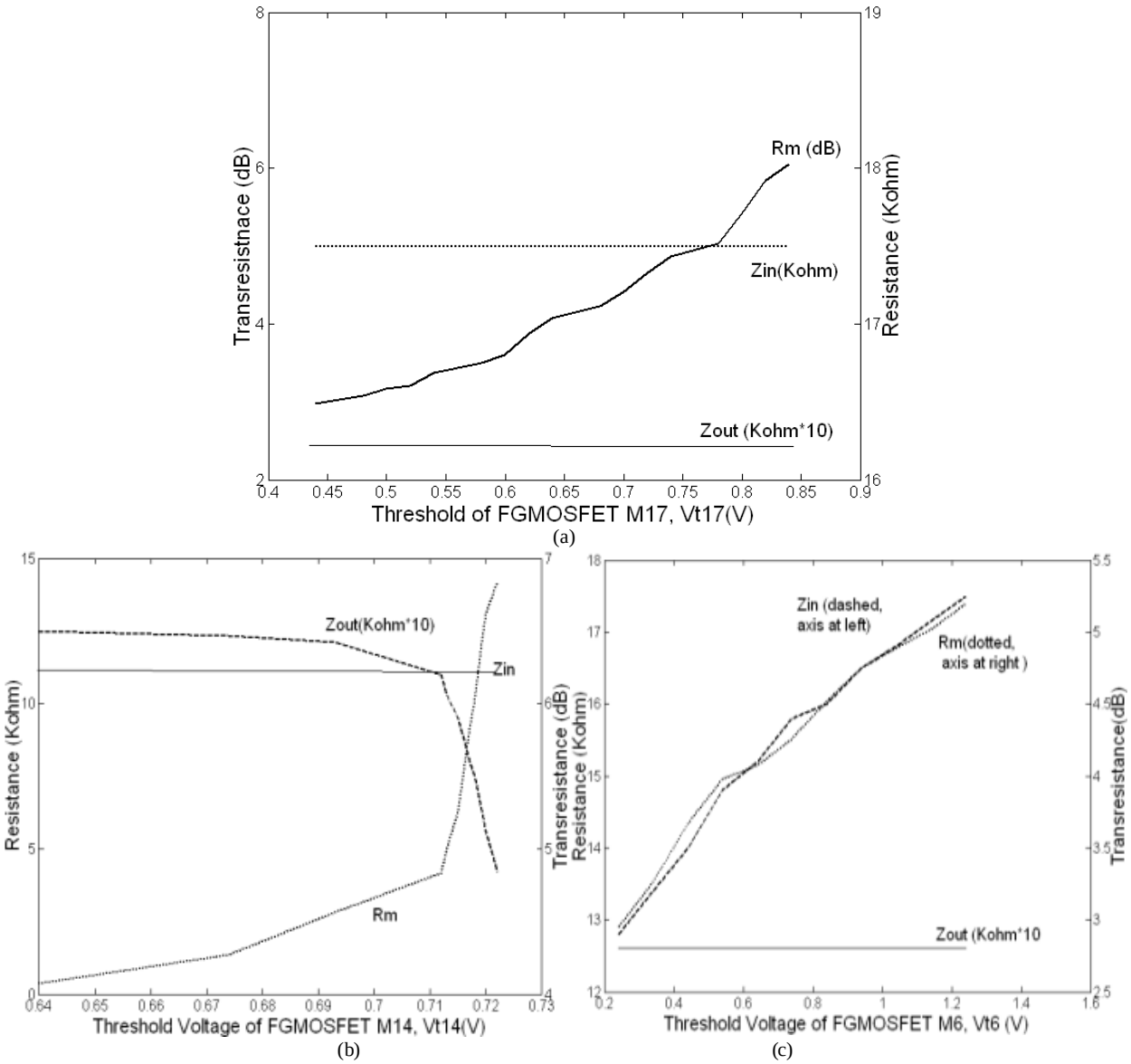
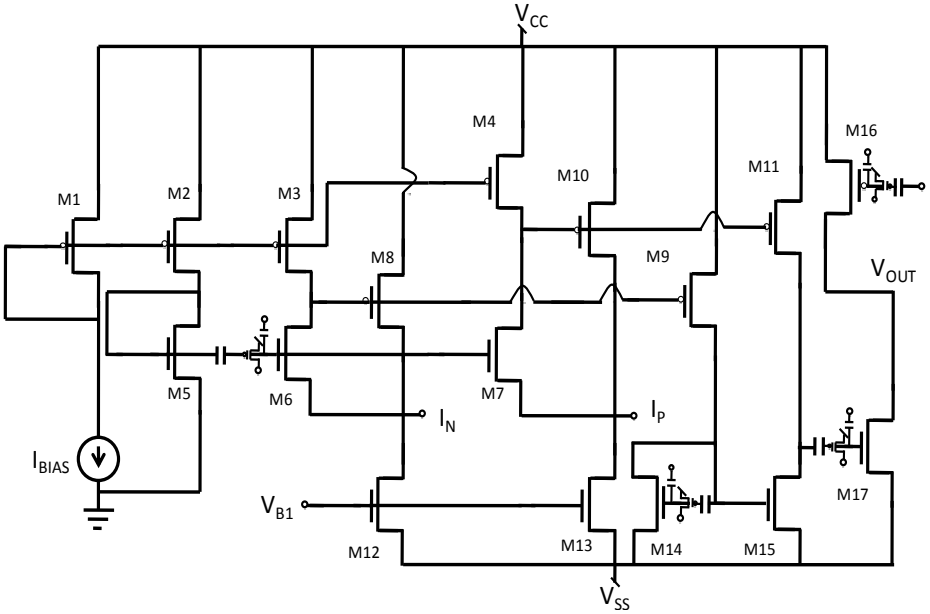


Figure 9. (a): The sensitivity analysis of all specifications w.r.t Vt17 (b): The sensitivity analysis of all specifications w.r.t Vt14 (c) The sensitivity analysis of all specifications w.r.t Vt6

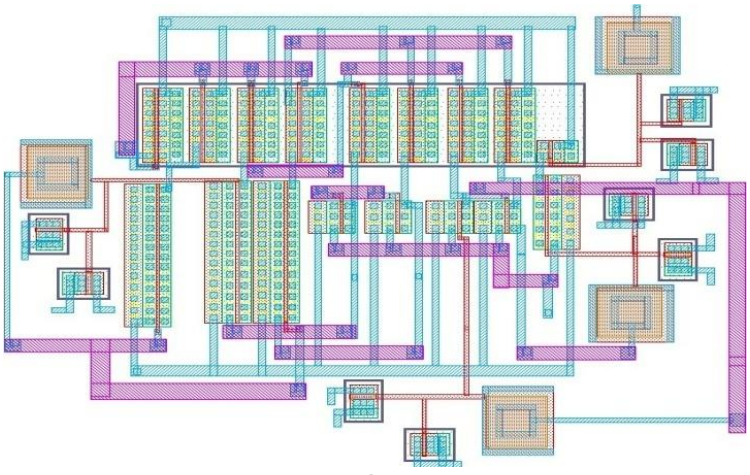
Table 3. Programming steps to program specifications along with their range of variation

Characteristics of OTRA	Range	Programming Steps
Transresistance Magnitude (Rm)	2 dB to 8dB (0.5kohm-6kohm) (can program independently with 13 bit resolution)	Transresistance magnitude is programmed independently with FGMOS M17, Vt17. No change in input output impedance, transresistance phase and even offset voltage.
Input resistance (Zin)	Initial value is fixed at 22.139 ohm but can program independently the input impedance at central frequency in range:10K– 20K(can program using M6 along with M17 with13-bit resolution)	Input impedance is programmed with FGMOS M6, Vt6 while transresistance magnitude is compensated using FGMOSFET M17, Vt17. No change in output impedance and in offset voltage.
Output Impedance (Zout)	350ohm to 125Kohm (can program using M14 along with M17 & M16 with 13-bit resolution) (not accurate)	Output impedance Zout is programmed with FGMOS M14, Vt14 while transresistance magnitude is compensated using FGMOSFET M17, Vt17, and offset voltage can be compensated using FGMOS M16, Vt16 (but have to adjust Zout).
Offset voltage (Vout) when In and Ip =0 (uA)	-1V to -2.8V (can program using M16 along with M14 with 13-bit resolution) (not accurate)	Offset voltage varies with almost all FGMOS programming but can be adjusted to specific value using FGMOS M16, Vt16 while Zout need to be compensated using FGMOS M14, Vt14

4.3. Final OTRA Circuit with Required Floating Gate Transistors and its Programming Steps



(a)



(b)

Figure 10. (a) Schematic of final modified Field Programmable High frequency OTRA developed using BSIM 3 level 49 models in Virtuoso (Cadence analog designer tool) 0.35 µm CMOS process using only four FGMOSs. (b) Layout of final OTRA circuit in which transresistance, input output impedance and offset voltage can be programmed independently using FGMOSs (M17, M14 and M6 respectively), which in turn can be programmed using two pFETs (mos capacitor for tunnelling and programmer PMOS for injection) at common floating gate, using external control voltages Vtun and Vinj, whereas, the charge at the floating gate can be stored at capacitor (160pF), placed between gate and floating gate of the floating gate transistor

The final modified programmable OTRA circuit using only three floating gate transistors M17, M6 and M14, is simulated using BSIM3 level 49 MOSFETs model along indirectly programmable FGMOS's simulation model using Virtuoso, 0.35 um CMOS process, as shown in Figure 10(a). The design is also being developed for fabrication and the layout is demonstrated in Figure 10 (b). The chip area occupied by the circuit is 75 µm × 64 µm. Thus circuit specifications of modified high frequency operational transresistance amplifier after fabrication to desired value in the specific range using respective floating gate transistors as expressed in form of programming steps in Table 3. Moreover, the specifications can be programmed with 13bit programming precision. Hence, circuit specifications can also be programmed continuously.

5. Conclusions

The proposed programmable OTRA design and final modified OTRA design are simulated and results claimed that the circuit specifications, transresistance, input impedance and output impedance can be programmed along with offset voltage compensation, using number of programming steps which can be executed with the help of floating gate transistor M17, M14 M6 and M16. All three design objectives, variation in the specifications should be large and continuous, variation of each specification should be independent of the other and operating point of the circuit should not alter too much during programming, i.e. offset current should not vary significantly have been justified from our results. Therefore, we would like to conclude by proposing OTRA in which transresistance, input impedance and output impedance can be programmable after fabrication. It finds applications in high frequency systems where field programmable current conveyor is required and justifies a systematic approach to develop programming ability in basic analog building blocks using non-volatile, indirect field-programming ability feature of floating gate transistors. Hence it can be used in RF programmable current-mode systems which require low power, thermally stable yet compact and simple hardware such as universal filters, square/triangular wave generators, current controlled sinusoidal oscillators, monostable multivibrator.

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