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Symmetric DG-MOSFET With Gate and Channel Engineering: A 2-D Simulation Study

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Abstract The present work is the study on the performance value of Double Gate (DG) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with different channel and gate engineering. Six different structures have been proposed and analysed keeping channel length constant. The short channel parameters like sub threshold swing (SS), transconductance (g_m), electric field, leakage current (I_{off}), electron mobility (μ_n) and drain induced barrier lowering (DIBL) are analysed and compared between Gate Stack Double Gate (GS-DG), GS-DG-Single Halo (SH), GS-DG-Double Halo (DH), GS-DG Tri-material (TM), GS-DG TM-SH and GS-DG-TM-DH MOSFETs. This work extensively provides the device structures which may be applicable for high speed switching and low power consumption application. In addition, the effects of gate misalignment on source/drain, device characteristics and various short channel parameters have been discussed and analysed. The simulation and parameter extraction have been done by using the commercially available device simulation software ATLAS^{TM}.

Keywords DG-MOSFET, Gate Stack, Single & Double Halo, SS, Short Channel Effects (SCEs), Device Simulator

1. Introduction

Traditional downscaling device technologies have been serving the microelectronic industry over the last three decades. Scaling with new materials & new device structures are now continually improving the performance of device technologies[1-4]. DG-MOSFETs seem to be a very promising candidate owing to its excellent SCEs suppression, higher drive current and transconductance, lower leakage current, better DIBL and better scaling capability compared to the bulk MOSFETs[5-9]. Now efficient Gate Engineering & Channel Engineering for sub-100-nm MOS devices is a major challenge[10].

Symmetric dual material & Triple-material gate structures for a DG-MOSFET have better immunity against SCEs[11-15]. In TM-DG MOSFETs, the gate electrode of the device consists of three laterally contacting materials with different work functions. Work function of the material near the source is highest and that near the drain is the lowest for n-channel MOSFETs (the opposite for p-channel). The high work function near the source leads to more rapid acceleration of carriers in the channel and the low work function near the drain leading to reduction in peak electric field at the drain side.

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However, continual gate oxide scaling requires high k gate dielectric; since the gate oxide leakage increases with reduced physical thickness of gate oxide (SiO_2). In order to suppress the gate leakage current with continuous thinning of gate oxide layer, gate oxide stack with high-k materials in the oxide region have been proposed[16]. The high -k gate stack also improve SCEs, DIBL and hot carrier effects, reduced channel length modulation, drain conductance and advance drive current in sub-100 nm regime[17-18].

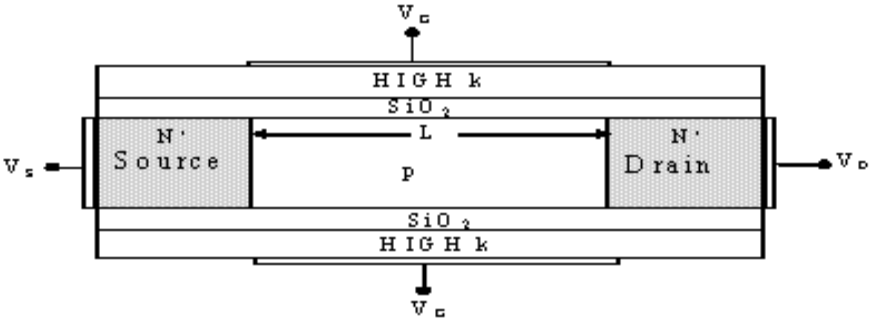
However, for channel lengths below 100 nm, DG MOSFETs still exhibits considerable leakage currents and to overcome this effect, different channel engineering techniques are used. In the past few years, the local high doping concentration in the channel near source/drain junctions have been implemented via lateral channel engineering, e.g. halo or pocket implants. Single halo MOSFET structures have been introduced for bulk as well as for SOI MOSFETs[19-24] to adjust the threshold voltage and to improve the device SCEs.

In this paper, GS is considered for all the device structures. GS-DG and GS-DG-TM are compared by taking DH (lateral symmetric channel) & SH (lateral asymmetric channel) techniques. In these structures, the channel is highly doped near the source & drain regions to reduce the width of the depletion region in the vicinity of the junctions. In effect, this reduces sub threshold leakage current and increases output impedance. The gate work-function engineering allows the GS-DG-TM devices to have the same threshold voltage for a reduced doping concentration in the channel region resulting

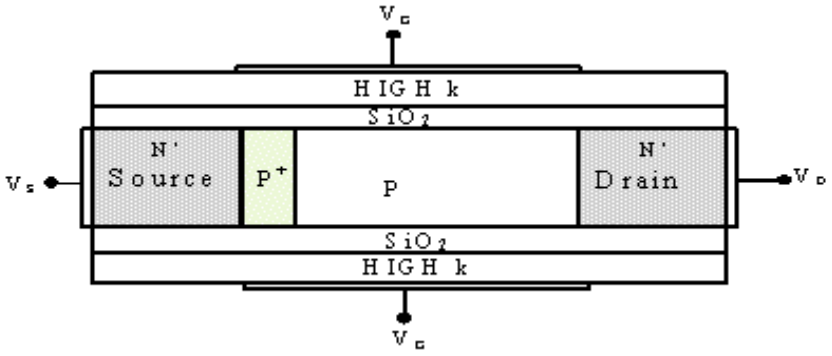
in better immunity to mobility degradation and hence higher transconductance. The characteristics of the GS-DG-TM device are compared with SH & DH doped SOI MOSFETs. This work also highlights one out of the various gate misalignments and its effect on source/drain, device characteristics and various short channel parameters have been discussed and analysed. In this paper, a model for the nanoscale fully depleted symmetrical GS-DG-TM-MOSFET is successfully simulated and studied.

2. Device Structure

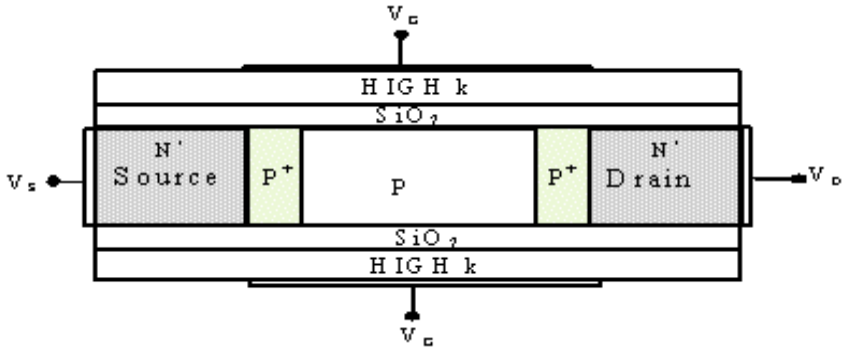
Figure 1.(a)-(f) shows the schematic cross-sectional view of the DG-MOSFETs (n-channel) with different structural models implemented in the 2D device simulator. In the structures, the channel length (L) and Source/Drain length (L_S/L_D) is kept as 40nm. The silicon thickness (T_{Si}) as 10nm and a uniform density N_D as 10^{20} cm^{-3} is taken. The channel is doped with impurity concentration of $N_A=10^{16}$ cm^{-3}. In each case the effective oxide thickness is 1.1625nm. The thickness of SiO_2 and equivalent HfO_2 are 1nm, 0.1625nm respectively. To get equivalent thickness of the high-k as 0.1625nm, the physical thickness is calculated as 1nm according to $EOT = T_k(k_{SiO2}/k_{high-k})$, where T_k is the physical thickness of high-k, k is the permittivity of dielectric material. The work function for the gate electrode is assumed as 4.8ev for single material DG-MOSFETs. The channel engineering SH and DH was implemented in GS-DG models in a ratio of 1:4 and 1:2:1 respectively with $N_A= 10^{18}$ cm^{-3} as shown in Figure 1(b) &(c). The control gate M1 (toward the source side) and screening gates M2 and M3 (toward the drain side) are the gate electrodes with lengths LM1, LM2 and LM3 (LM1: LM2:LM3 = 1:2:1) and with metal work functions qφM1, qφM2 and qφM3 (4.8ev, 4.6ev &4.4ev).



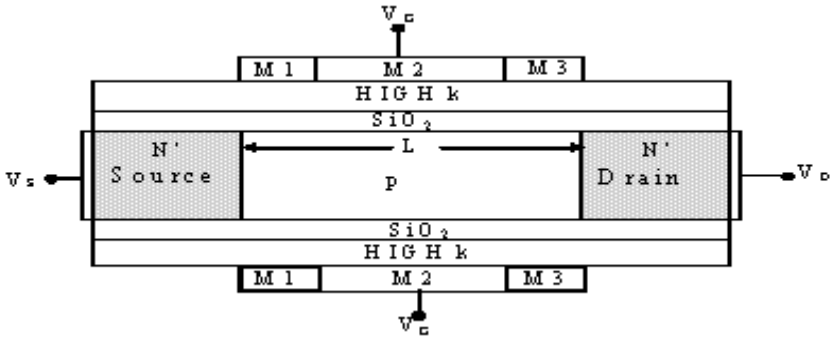
(a) GS-DG



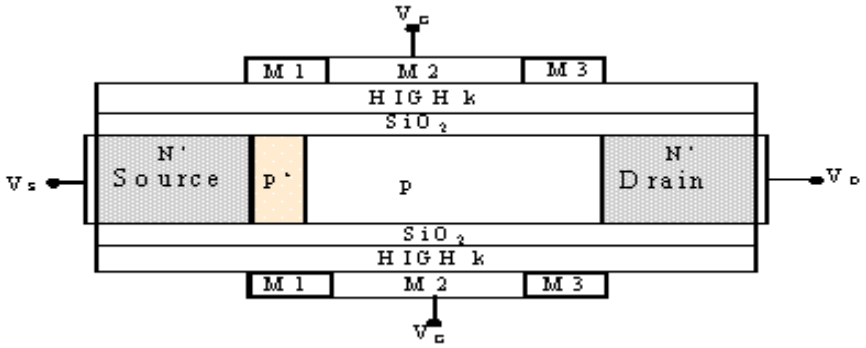
(b) GS-DG-SH



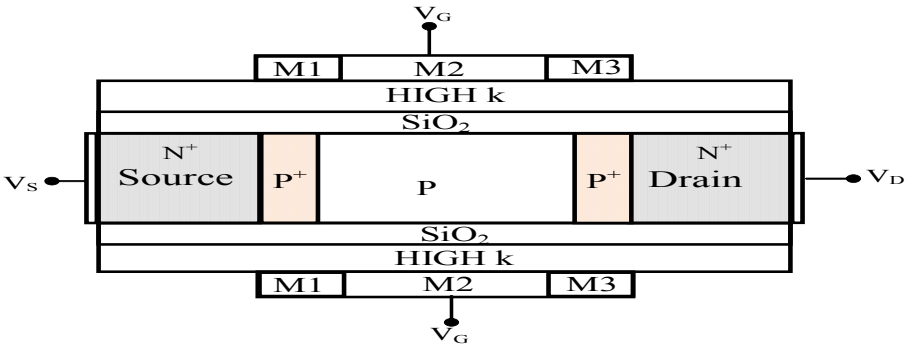
(c) GS-DG-DH



(d) GS-DG-TM



(e) GS-DG-TM-SH



(f) GS-DG-TM-DH

Figure 1. Schematic structures of DG-MOSFETs with (a) GS-DG (b) GS-DG-SH (c) GS-DG-DH (d) GS-DG-TM (e) GS-DG-TM-SH (f) GS-DG-TM-DH

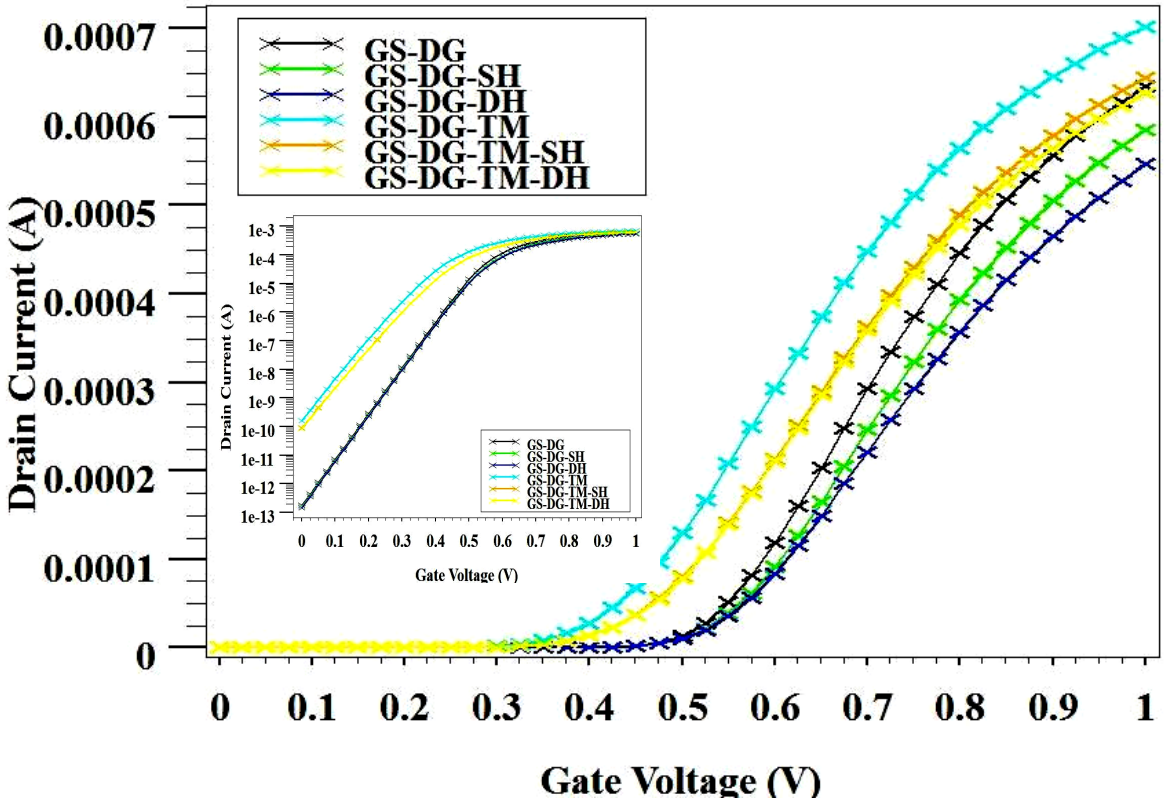
3. Simulation

To obtain accurate results for MOSFET simulation we need to account for the mobility degradation that occurs inside inversion layers. The degradation normally occurs as a result of higher surface scattering near the semiconductor to insulator interface. So, in the simulation, the inversion-layer Lombardi constant voltage and temperature (CVT) mobility model is used, that takes into account the effect of transverse fields along with doping and temperature dependent parameters of the mobility. The Shockley–Read–Hall (SRH) model simulates the leakage currents that exist due to thermal generation. Electrons in thermal equilibrium at given temperature with a semiconductor lattice obey Fermi-Dirac statistics. The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials. The model Fermi-Dirac uses a Rational Chebyshev approximation that gives results close to the exact values. The Auger recombination models for minority carrier recombination have been used. Furthermore, we chose Gummel's method (or the decoupled method) which performs a Gummel iteration for Newton solution[25].

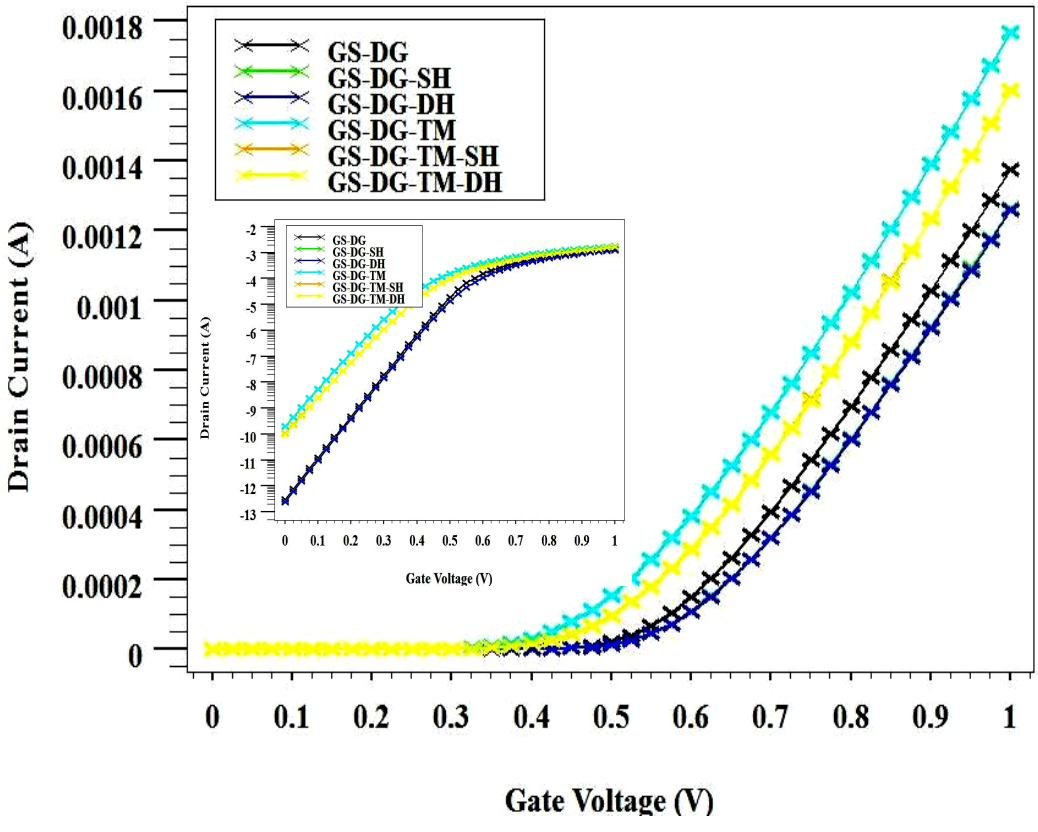
3. Results & Discussion

3.1. Aligned Gate

In Figure 2 (a),(b) I_{DS}-V_{GS} transfer characteristics have been shown on linear scale and log scale for all six different device structures and have been compared for V_{DS}=10 mV and 1.2 V. The GS-DG-TM provides higher drain current in comparison to all other configurations. The halo doping on both, the source and drain end, show a lower drain current because higher doping concentration reduces the surface mobility.



(a)



(b)

Figure 2. Drain Current (I_D) in both linear and log scale(inset) as a function of Gate Voltage (V_{GS}) at (a) V_{DS} =0.1V (b) V_{DS} =1.2V for all models

Furthermore, as shown in Table 1, the sub threshold slope SS is lower for GS-engineered devices, i.e., GS-DG-SH and GS-DG-DH. However, the GS technology, along with the TM gate technology i.e., GS-DG-TM-SH and GS-DG-TM-DH, increases the sub threshold slope. This is because, in the TM architecture, there is a small drain voltage drop across the drain side of the channel due to lower work-function of the gate. Thus, more V_{DS} drop occurs across the source side of the channel leading to higher short channel effects.

$$V_t = V_{fb} + \varphi_{st} + \sqrt{qN_{sub}\,2\epsilon_s\varphi_{st}}/C_{ox} \quad (1)$$

From the relation (1) the threshold voltage is directly related to the body doping. So, the threshold voltage is somewhat more for halo implanted structures as compared to others because of the variation in doping profile as given in Table 1.

$$I_{off}(nA) = 100.W/L.10^{-V_t/SS} \quad (2)$$

From the above relation, in order to minimize the off current either we can increase the threshold voltage or decrease the SS value. Therefore, a little increase in threshold voltage give rise to low off current for the same halo implanted structures which are given in Table 3.

$$SS(mV/decade) = \eta.60mV.T/300K \quad (3)$$

$$\eta = 1 + C_{dep}/C_{ox} \quad (4)$$

$$W_{dep} = \sqrt{2\epsilon_s\varphi/qN_A} \quad (5)$$

In addition, as can be seen from all the above three relations, the high doping is a major problem for the SS value. As doping (N_A) increases, W_{dep} decreases, C_{dep} increases and there is an increase in η value which consequently leads to an increase in SS value.

The g_m versus V_{GS} characteristics have been compared for all six device structures in Figure 3 for V_{DS}=0.1V and 1.2V. As we know:

$$g_m = \frac{dI_D}{dV_{GS}} \quad (6)$$

The value of g_m is extracted by taking the derivative of I_D-V_{GS} curve, the values of which are summarized in Table 1 and Table 2. From the extracted data, it can be examined that the GS-DG configurations give higher g_m values and also a higher drain current. According to the relation in equation 1, g_m is directly related to the drain current (I_D).

Figure 4 & 5 shows the simulated electron mobility and electric field profiles along the channel position for various configurations at V_{DS}=0.1V and 1.2V. In the GS-TM technology, the work function difference between M_1, M_2 and M_3 causes an abrupt change in the conduction band energy at the silicon surface. This generates two steps in the electric field peak profile which give rise to two peaks in the channel with a high electric field at the source side. Thus, for the GS-DG-TM MOSFETs, the electric field at the drain end is reduced and the source carrier injection into the channel is enhanced. But the models with halo doping gives high electron mobility as they show low electric field in the channel region because electron mobility is inversely proportional to the electric field.

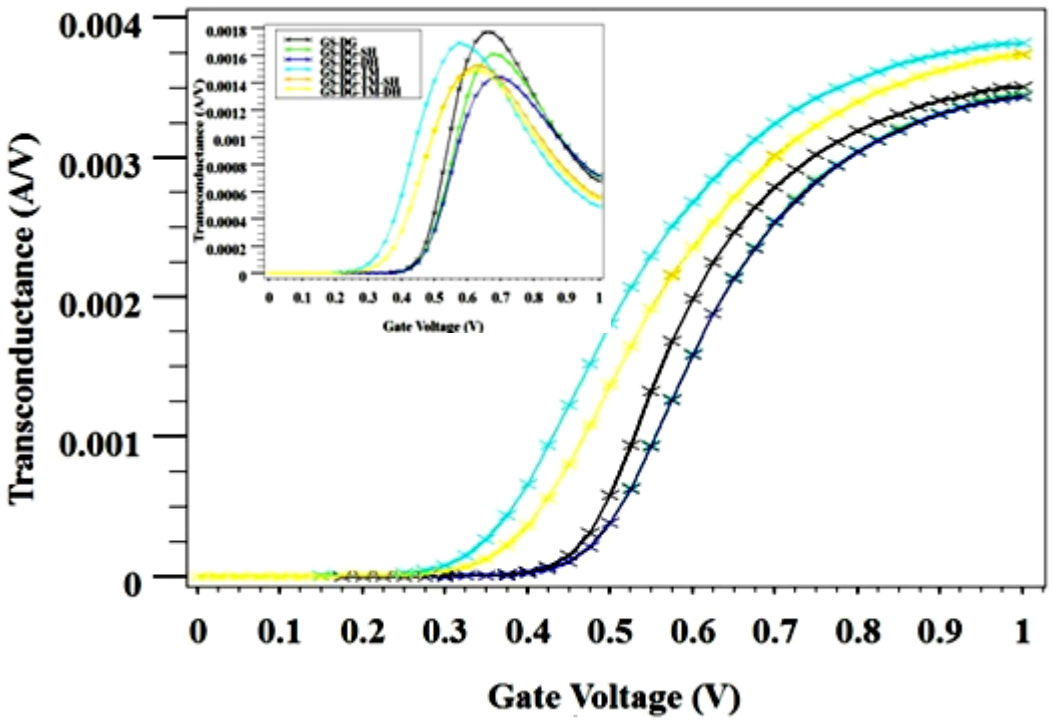


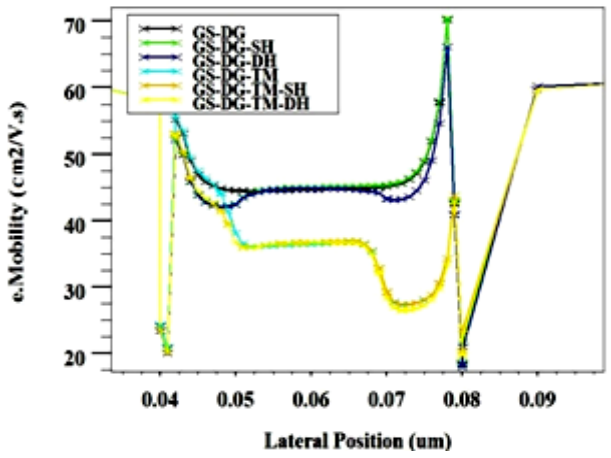
Figure 3. Variation of g_m as a function V_{GS} at V_{DS} =0.1V (inset) and V_{DS} =1.2V for all structures

Table 1. Extracted Parameters at V_D=0.1V, Vg=0V-to-1.2V

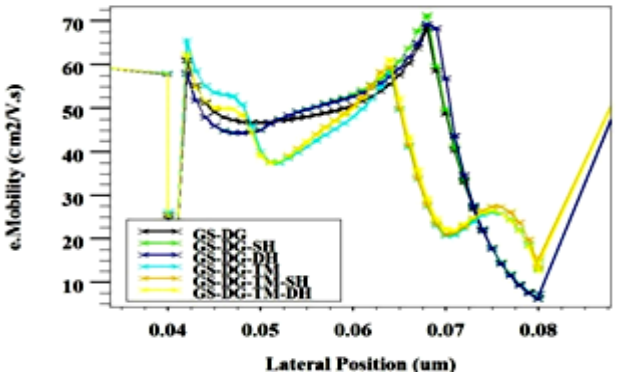
Device Structure	Name	V_{t1} (V)	SS_1 (mV /Decade)	G_{m1} (mA/V)	I_{on1} (mA)
GS - DG	D-1	0.49	62.14	1.78	0.63
GS - DG- SH	D-2	0.50	62.19	1.62	0.59
GS - DG- DH	D-3	0.50	62.17	1.45	0.55
GS - DG- TM	D-4	0.38	67.86	1.69	0.70
GS - DG- TM-SH	D-5	0.41	70.33	1.53	0.64
GS - DG-TM-DH	D-6	0.41	70.25	1.50	0.63

Table 2. Extracted Parameters at V_D=1V, Vg=0V-to-1.2V

Name	V_{t2} (V)	SS_2 (mV /Decade)	G_{m2} (mA/V)	I_{on2} (mA)
D-1	0.11	62.33	3.51	1.37
D-2	0.13	62.50	3.45	1.26
D-3	0.13	62.42	3.44	1.26
D-4	0.04	68.27	3.82	1.77
D-5	0.07	70.63	3.74	1.60
D-6	0.07	70.57	3.73	1.60

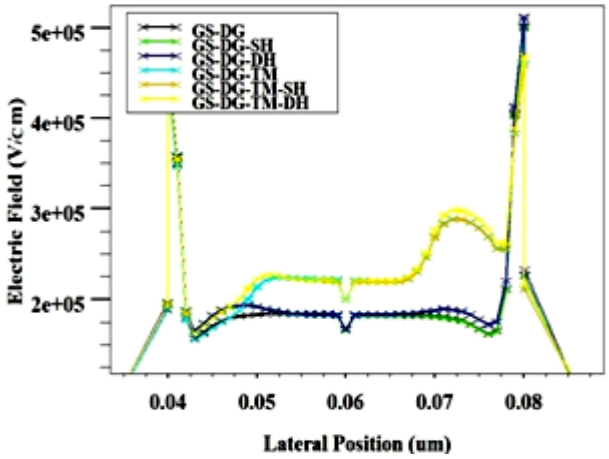


(a)

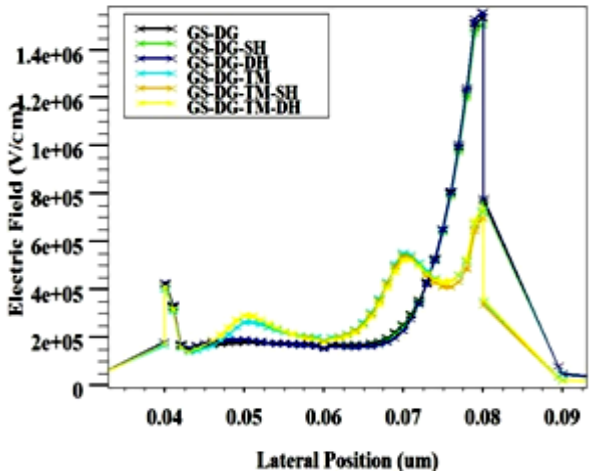


(b)

Figure 4. Electron Mobility along the channel (cutline at Y=4nm) (a) at V_{DS}=0.1V and (b) at V_{DS}=1V for different models



(a)



(b)

Figure 5. Electric Field along the channel (cutline at Y=4nm) (a) at V_{DS}=0.1V and (b) at V_{DS}=1V for different models

Figure 6 (a), (b) & (c) shows the leakage current, threshold voltage and transconductance variation for all device configurations. The off state current (I_{off}) is extracted by calculating the drain current (I_D) at V_{GS}=0 and V_{DS}=V_{DD}. The I_{off} for all six device structures is summarized in Table 3. It is important to keep I_{off} very small in order to minimize the static power dissipation when the device is in off state.

Table 3. Extracted Parameters (DIBL and I_{off})

Device Structure	I_{off1} (pA)	DIBL (mV/V)
GS - DG	0.40	343.21
GS - DG- SH	0.39	330.84
GS - DG- DH	0.39	330.34
GS - DG- TM	165.00	309.54
GS - DG- TM -SH	89.28	308.88
GS - DG- TM -DH	88.17	306.79

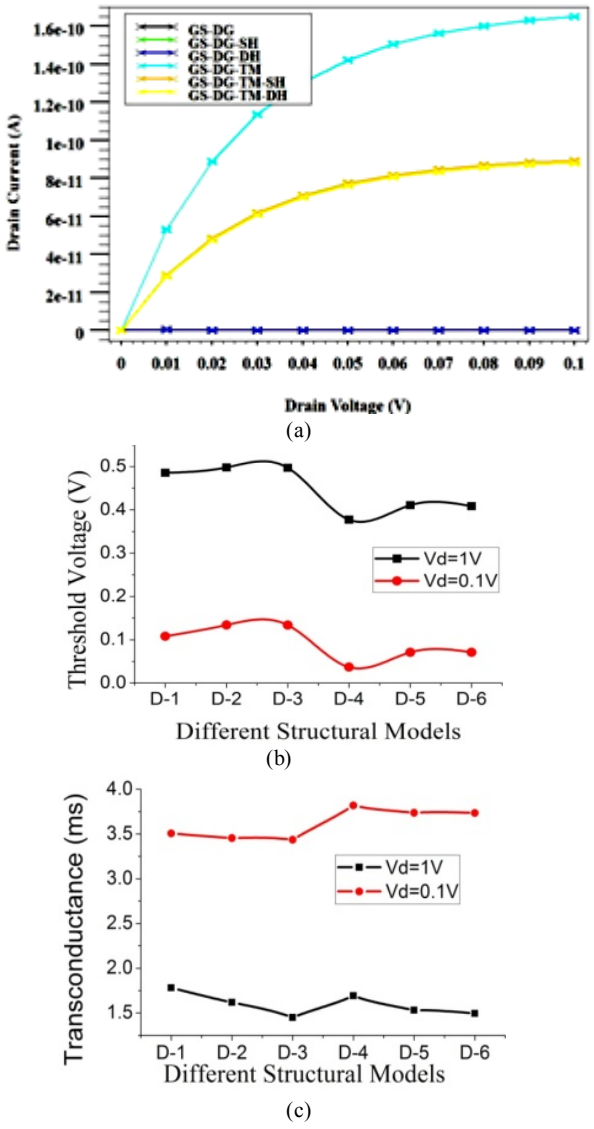


Figure 6. (a) Curve of Leakage Current (I_{off}) as a function of V_{DS} at V_{GS} =0V, (b) & (C) Threshold Voltage (V_t) and Transconductance (G_m) variation of different models

As we know: DIBL = $\Delta V_{th} / \Delta V_d$

The DIBL calculated as V_{th} at V_D=0.1 V and V_D=1.2 V. The GS-DG-TM model shows lower DIBL values as compare to other structures owing to its low value of V_{th}.

3.2. Misalignment of Gate

The fabrication of planer DG-SOI in the sub-100 nm regime with an ideal self-aligned structure is very difficult. The Source/Drain asymmetric effects are produced by the Gate misalignment. Understanding the Source/Drain effects and how to deal with them is very essential. Therefore, in this section, we have analyzed the Source/Drain asymmetry caused by gate non-overlapping. Apart from many possible gate misalignments, here one typical case has been taken into consideration. In this case, it is assumed that the top gate is shifted towards the drain side and bottom gate towards the source side 10nm each.

In Fig.7 & 8, the transfer characteristic and transconductance are shown for all the device structures and have been compared for V_{DS}=10 mV and 1.2 V by considering gate misalignment effects. All the possible parameters are extracted from the above figures and a comparison is being made between them as highlighted in Table 4 & 5. By comparing the parameters with the previous parameters that are already discussed in Table 1 & 2 we conclude that there are many effects occurring because of the gate misalignment. The non-ideal effects introduced by gate misalignment can be either from the non-overlapping region or from the overlapping region. In this structure, the non-overlapping region is located towards the drain, so the bottom channel near the drain is weakly controlled by the bottom gate. As a result, the drain potential can easily extends toward the channels through the bottom part of channel region.

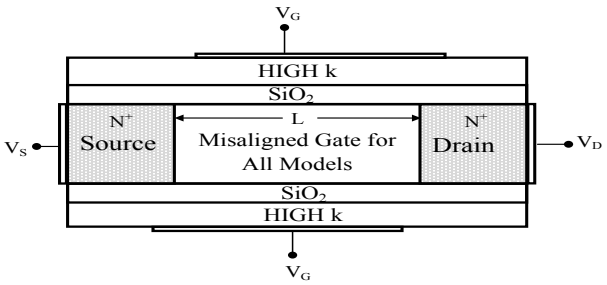


Figure 7. Misaligned gate for all models

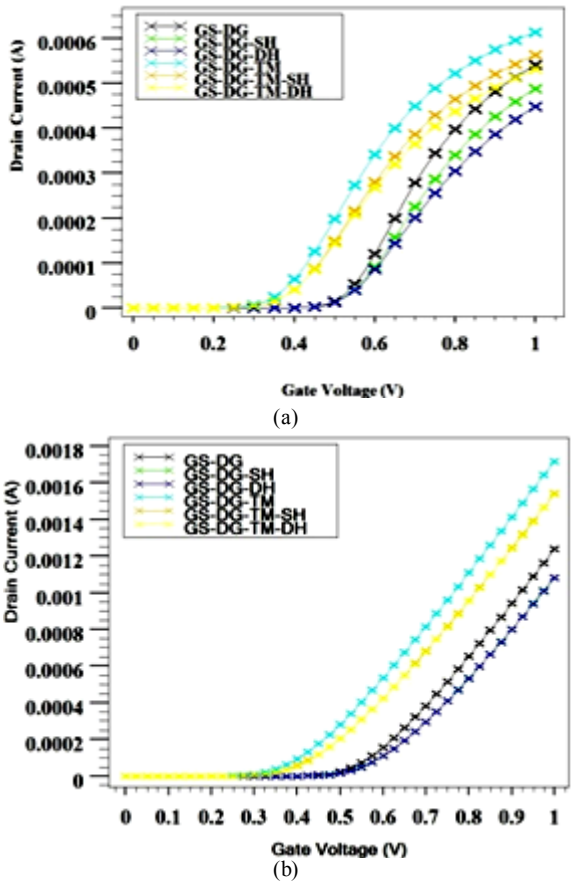
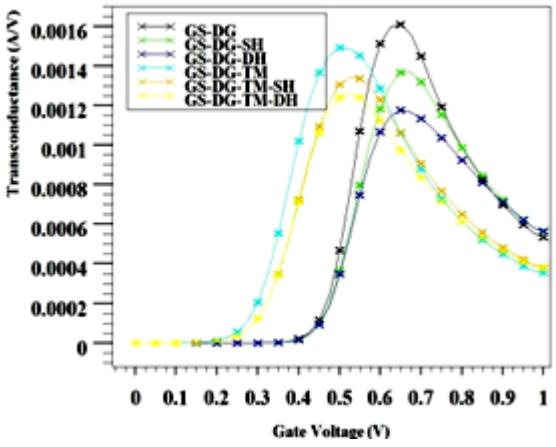
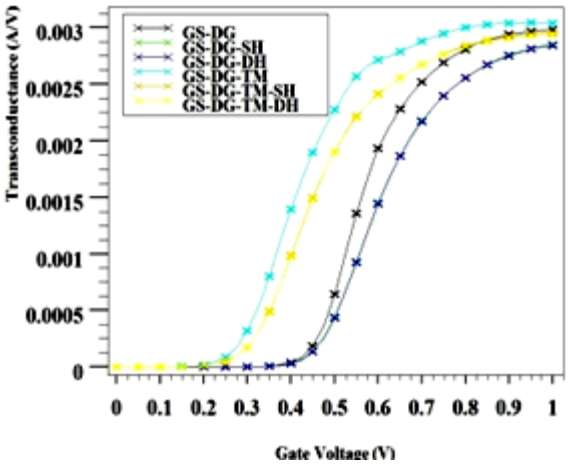


Figure 8. Drain Current (I_D) as a function of Gate Voltage (V_{GS}) at (a) V_{DS} =0.1V (b) V_{DS} =1.2V for all models with one typical misaligned gate



(a)



(b)

Figure 9. Variation of g_m as a function V_{GS} at (a) V_{DS} =0.1V (b) V_{DS} =1.2V for all structures with one typical misaligned gate

Table 4. Extracted Parameters misaligned gate at V_D=0.1V, Vg=0V-to-1.2V

Device Structure	Name	V_{t1} (V)	SS_1 (mV /Decade)	G_{m1} (mA/V)	I_{on1} (mA)
GS - DG	D-1	0.48	63.47	1.62	0.54
GS - DG- SH	D-2	0.49	63.48	1.38	0.49
GS - DG- DH	D-3	0.48	63.44	1.18	0.45
GS - DG- TM	D-4	0.32	67.72	1.50	0.61
GS - DG- TM-SH	D-5	0.34	68.45	1.35	0.56
GS - DG-TM-DH	D-6	0.34	68.35	1.26	0.53

Table 5. Extracted Parameters misaligned gate at V_D=1V, Vg=0V-to-1.2V

Name	V_{t2} (V)	SS_2 (mV /Decade)	G_{m2} (mA/V)	I_{on2} (mA)
D-1	0.09	63.85	2.98	1.24
D-2	0.12	64.00	2.85	1.08
D-3	0.12	63.92	2.84	1.08
D-4	-0.06	68.07	3.04	1.72
D-5	-0.02	68.82	2.95	1.54
D-6	-0.02	68.77	2.94	1.54

4. Conclusions

A close comparison of various design engineering such as the channel and gate engineering on the DG-SOI MOSFETs are studied. The GS engineering along with the halo implantation i.e. GS-DG-SH and GS-DG-DH configurations have demonstrated significant improvements in the device characteristics such as SS value, electron mobility and leakage current. On the other hand by applying gate engineering with halo implantation i.e. GS-DG-TM-SH and GS-DG-TM-DH exhibits a higher value of drain current, the peak transconductance and a lower value of DIBL. In addition, the gate misalignment and its effects on source and drain have also been discussed. The various characteristics and extracted short channel parameters considering gate misalignment have been analysed and a comparison is being shown between them. Therefore, the simulated models in this paper are promising candidates for high speed switching and low power consumption application provided the gate misalignment effects are taken into consideration while fabricating the device.

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