Macromodeling of Power VDMOSFET Transistor Incorporating Self-Heating Effect

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Abstract Self heating model simulation of power electronic semiconductors is now required in accurate optimisation of power electronic circuits and systems. This requires accurate, but not too complex, self heating models of power semiconductors to be used in commercially available power electronic circuit simulators. Realization of one such self-heating model for power VDMOSFET in PSPICE 10.5 is described in the paper. Model consists of electrical and thermal part with interactive exchange of variables. Self-heating model and standard model was tested on unclamped inductive circuit.

Keywords Power VDMOSFET, Device Modelling, Junction Temperature, Power Discrete Devices, Simulation, Spice, Unclamped Inductive Switching

1. Introduction

Today, circuit simulators are standard tools in the development and optimization of electronic systems. However, simulation has until now been limited to electronic functions because, in the simulation models available today, temperature dependence can at best be taken into account by changing the static global temperature. Inpower-electronic systems in particular, the temperature is one of the critical parameters due to the fact that many properties of power semiconductors are very strongly temperature-dependent – following are some examples:

1) A maximum junction temperature is specified for all semiconductor components[3],[8] which, when exceeded, can lead to destruction or permanent damage of the component. Even when temporary events such as avalanche or short-circuit conditions occur, it must be ensured that the maximum permissible junction temperature is not exceeded – a problem which is almost impossible to solve by conventional means, i.e. using a Zth-diagram.

2) Within the safe operating range, the lifetime of semiconductor components is strongly affected by temperature fluctuations due to loading. Each change in temperature causes mechanical stress in the component which, in particular, affects solder and bond connections. Here it is not the absolute temperature which is decisive but the temperature cycling. As a rule of thumb it can be assumed that the aging of a as a rule of thumb it can be assumed that the aging of a component is proportional to the fourth (!) power of the temperature deviation[1].

3) The ON-resistance of a MOSFET and thus the conduction losses are roughly doubled with a temperature increase from 25℃ to 150℃.

4) The threshold voltage of a MOSFET drops with increasing temperature which reduces the signal-to-noise margin at the control node. Ignoring this effect can lead to an undesired – even catastrophic – turn-on of the transistor when it should be inhibited, especially in bridge circuits with high slew rates for the drain-source voltage. In addition to these aspects, the question of the fluctuation in the junction temperature is also becoming more and more important in the course of circuit design. Some of the over dimensioning for example in the switching of lamps or motors to cover temporary overloads is no longer necessary when the brief, excessive power dissipation can be compensated by suitably coupled thermal capacitances. Similarly, this applies when one wants to do away with the usual protection circuits when relying on the high robustness of today's power semiconductors. Avalanche energy of modern power MOSFETs for example is specified in such a way that any load current pulse pattern below the rated current is allowed as long as it is ensured that the peak junction temperature does not exceed the maximum value. In order to be able to simulate the time-dependent temperature curves which occur in all operating states, it is necessary to couple the electrical model of a component dynamically with the description of its thermal properties. For use in an electric circuit simulator, the thermal description by an electric analog model is to be preferred.

The MOSFET model reference on which this work is based has been explained in[1]-[2]-[3]. The reader is encouraged to refer to these references for a full understanding of the MOSFET model parameters herein referred to as

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the standard SPICE MOSFET model. Recent works[8]-[9] have demonstrated methods of circumventing the SPICE global temperature definition, providing a means of using the device's own junction temperature as a self-heating feedback mechanism.

New model studied recently[10] has taken into account the statically behaviour. This paper presents a new version of the dynamical behaviour.
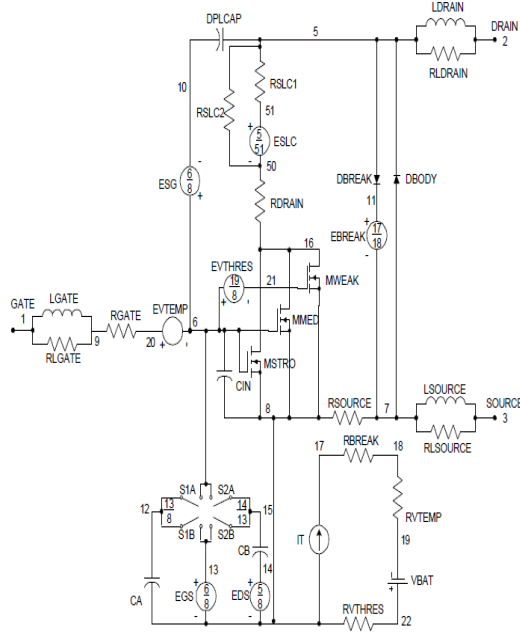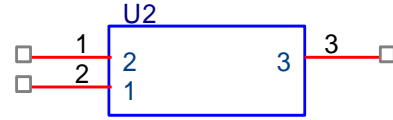
2. Standard SPICE MOSFET Model

Figure 1. Standard VDMOSFET Macro-model Dependent on Global Temperature Definition

The macro-model in Figure 1 is that used in many Fairchild MOSFET device models. It is the evolution of many years of work and improvements from numerous contributors[1]-[7]. A significant advantage of this model is that extensive knowledge of device physics or process details are not required for implementing parametric data within the model. The following data curves are the basis used to generate the macro-model model over temperature: transfer characteristic, saturation characteristic, Rds (on), gate threshold voltage, drain-to-source breakdown voltage, intrinsic body diode voltage, capacitance versus drain-to-source voltage, and gate charge waveform. Parametric data for up to five temperature points are used for model calibration resulting in a macro-model that provides representative simulation data for any rated operating junction temperature. The limitation of the standard MOSFET model is found in simulations involving severe pulsed power dissipation, and parallel operation. Reliance of the SPICE MOSFET primitive on the global analysis temperature variable (.TEMP SPICE instruction) results in simulations having all MOSFETs operating at a single predefined temperature. Device behaviour under high power dissipation transitory excursions cannot be accurately modeled. Threshold voltage and

Rds(on) are but two of the important parameters that can change sufficiently as to render a simulation inaccurate

VDMOSFET STANDARD MODEL

Figure 2.   Standard VDMOSFET PSPICE Symbol

3. Self-Heating Spice MOSFET Model

Improved implementation of static and dynamic behaviour is achieved with the self-heating SPICE MOSFET model (Figure 2), an evolution of the standard MOSFET model (Figure 1). Improved implementation of static and dynamic behaviour is achieved. Temperature dependent model parameters respond in closed loop form to the junction temperature information provided by node Tj. Performance is independent of SPICE's global temperature definition .TEMP, circumventing the level-1 NMOS model primitive self-heating limitation. All MOSFET operating losses are inclusive in the current source G_Pdiss (scaling of 1A = 1W dissipation) representing instantaneous power dissipation into the thermal model.

Multiple MOSFETs may be simulated at different and variable junction temperatures. Each MOSFET can be connected to a heat sink model via node Tcase. The heat sink model can be device specific, so heat sink optimization becomes possible. Current source G_Pdiss is referenced to the simulation ground reference, permitting use of the model in bridge topologies
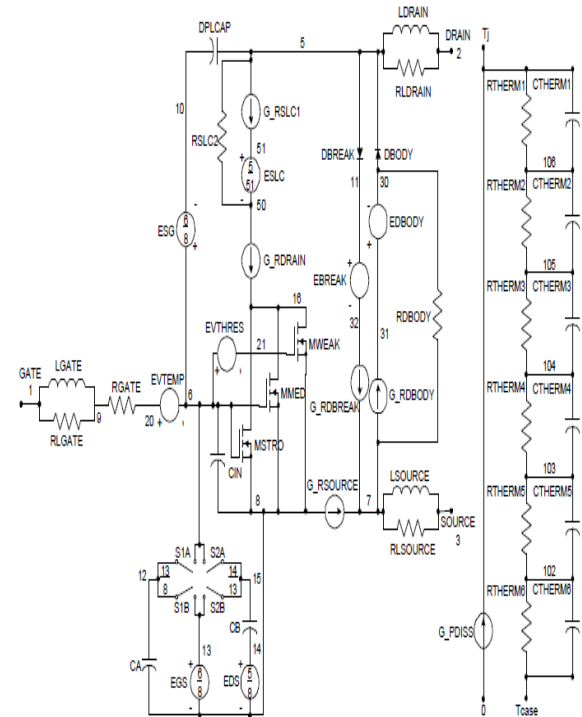

Figure 3. Self-Heating VDMOSFET Macro-model Independent of Global Temperature Definition

An example of a symbol representation of the self-heating MOSFET model is shown in Figure 3. Symbol files are available for OrCAD's two circuit entry tools "PSpice Schematic" and "OrCAD Capture". Recommended implementation of the symbol is to designate the pin out attribute for Tj as optional (ERC = DON'T CARE). Tj is the representation of the device junction temperature. It may be used as a monitoring point, or it may be connected to a defined voltage source to override the self-heating feature. Tcase must be connected to a heat sink model. Treatment of connections to the model's gate, drain, and source terminals are no different than those of the standard MOFET model.

U2

VDMOSFET SELFHEATING MODEL
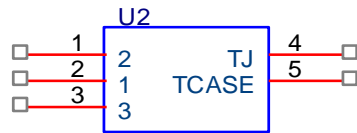
Figure 4.   Self-Heating VDMOSFET PSPICE Symbol

4. Self-Heating model Implementation

Ability to describe the value of a resistor and its temperature coefficients as a behavioural model referenced to a voltage node is necessary to express dependence on junction temperature. SPICE resistor ABMs do not permit voltage node references. Dynamic temperature dependence of the MOSFET's resistive element (expressed as separate lumped elements) and of the diode's resistive component cannot be implemented without a resistor behavioural model. This limitation is overcome by using a voltage controlled current source ABM expression (Figure 5). By using the nodes of the current source for voltage control, it becomes possible to express a resistor as a voltage-controlled current source by implementing the expression for the resistor's current as I = V/R (Tj). The resistance R (Tj) becomes a behavioural model expression dependent on the voltage node Tj representation of junction temperature. This voltage-controlled current source ABM model was used to modify the standard MOSFET model from Figure 1 by implementing voltage dependent versions of RDRAIN, RSOURCE, and RSLC1. Behavioural expressions were implemented in the self-heating model to eliminate IT, RBREAK, RVTEMP, and V_{BAT} through modification of EVTEMP, EVTHRES, and EBREAK.

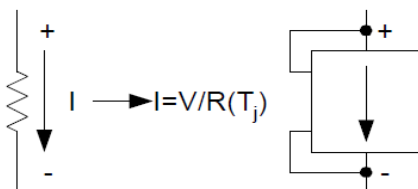**Figure 5.**   Implementing a Voltage Dependent ABM Resistor Model

Temperature dependent resistive elements of diodes DBODY and DBREAK were separated from the diode

model and expressed as voltage controlled current source ABM models G_R_{DBODY} and G_R_{DBREAK}. A large value resistor R_{DBODY} was added to improve convergence. ED$_{BODY}$ is added in series with D_{BODY} to incorporate the intrinsic body diode forward conduction drop temperature dependency. Junction temperature information is implemented by the inclusion of the thermal network $Z_{\theta JC}$ and current source G_P_{DISS}. The thermal network parameters are supplied in Fairchild data sheets. G_P_{DISS} calculates the MOSFET instantaneous operating loss, and expresses the result in the form of a current using the scaling ratio of 1A=1W. This is a circuit form implementation of the junction temperature from expression (1)

$$T_J = P_{Dissipation} . Z_{\theta JC} + T\ case \qquad (1)$$

Where T_J = junction temperature, $P_{Dissipation}$ = instantaneous power loss, $Z_{\theta JC}$ = thermal impedance junction-to-case and Tcase = Case temperature. Tj and Tcase use the scaling factor $1V = 1^{o}C$.

5. Simulating Unclamped Inductive Switching

The unclamped inductive switching (UIS) test circuit in Figure 6 was used to compare the performance of the VDMOSFET (3.5 mΩ, 60V, TO-263) self-heating MOSFET model with that of the standard model and measurement results.
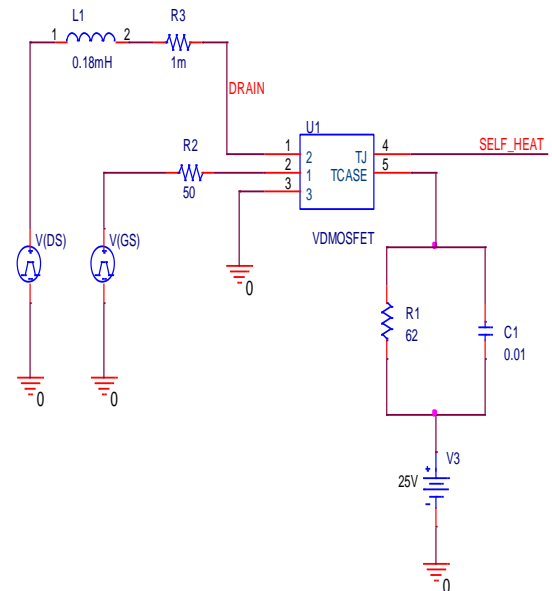
Figure 6.   UIS circuit used in the simulation

The standard MOSFET model unclamped inductive switching simulation results were performed with PSPICE TNOM and .TEMP variables set to 25℃ (Figure 6). The lack of temperature feedback to the model results in a drain-source breakdown voltage that is strictly drain current
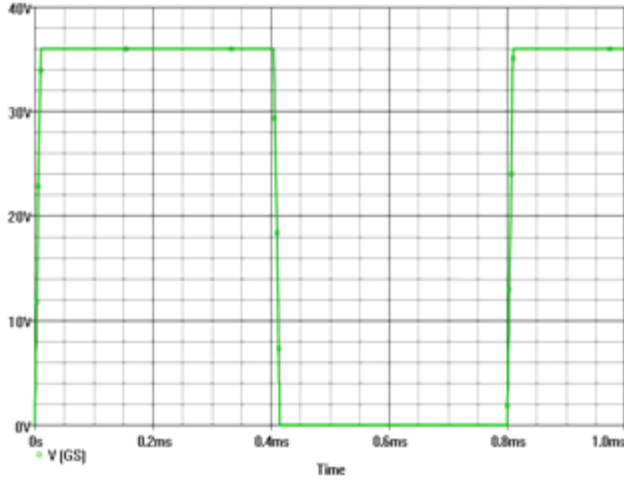
dependent.
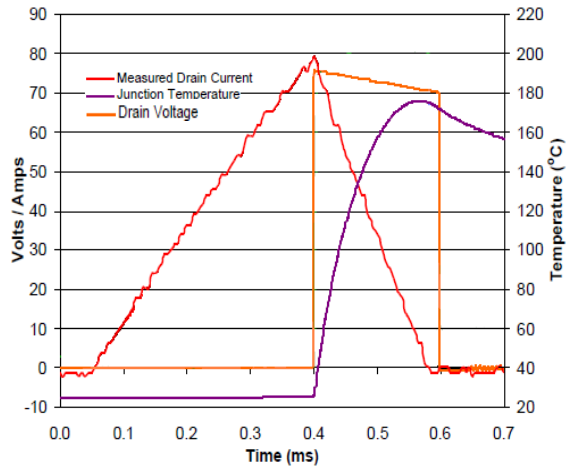

Figure 7.   Waveform of the gate voltage V_G (V)

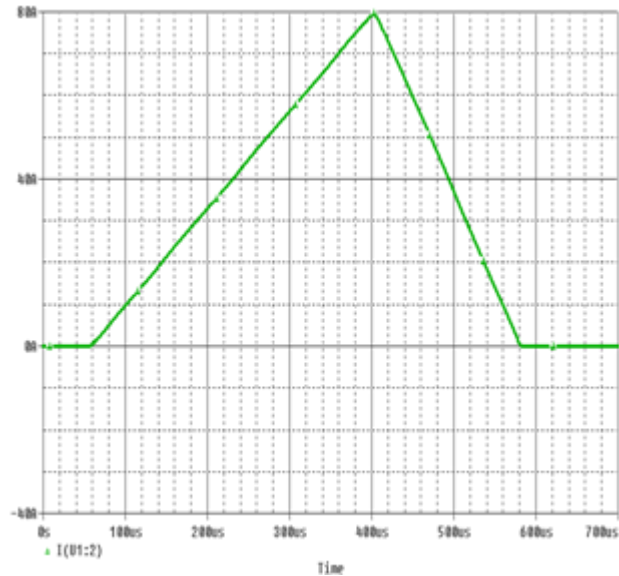**Figure 8.**   Measured UIS waveforms for a VDMOSFET standard model

Figure 8a.   Simulated drain current (I_{DRAIN}) for the VDMOSFET transistor

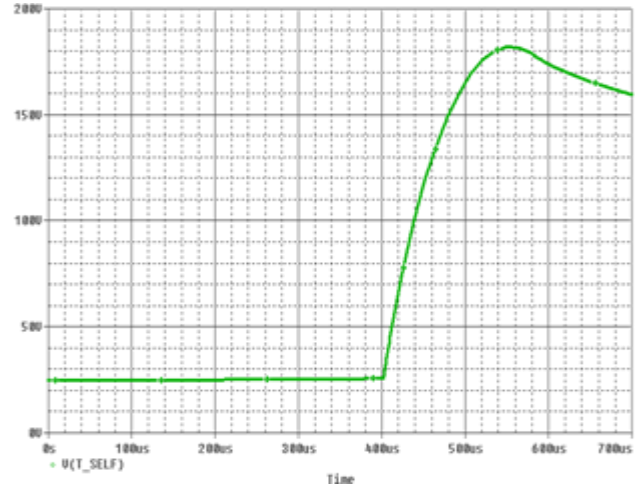**Figure 8b.**   Simulated drain voltage (V_{DS}) for the VDMOSFET transistor

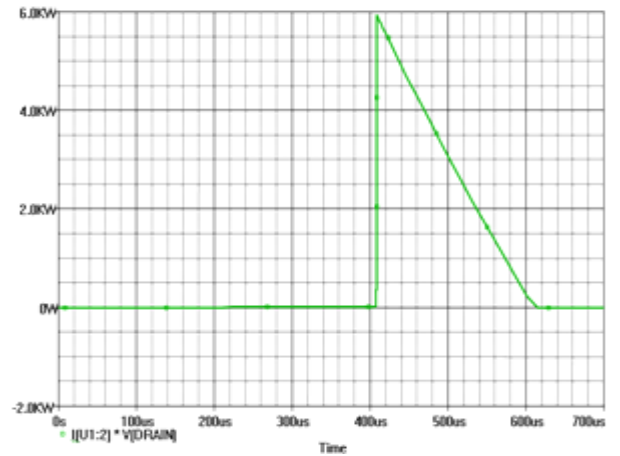**Figure 8c.**   Simulated junction temperature ($V_{SELF-HEATING}$) (1V=1℃)

Figure 8d.   Simulated power loss (I_{DRAIN}*V_{DRAIN}) of the VDMOSFET standard model
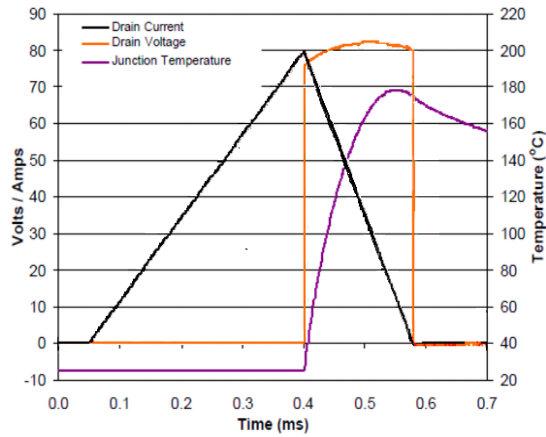
Figure 9. Measured UIS waveforms for a VDMOSFET Self-Heating Model

Unclamped inductive simulation results for a self heating MOSFET model are shown in Figure9. (a, b, c, d). Simulated drain-source breakdown voltage demonstrates the model dependence on junction temperature as well as drain current. Excellent agreement exits.
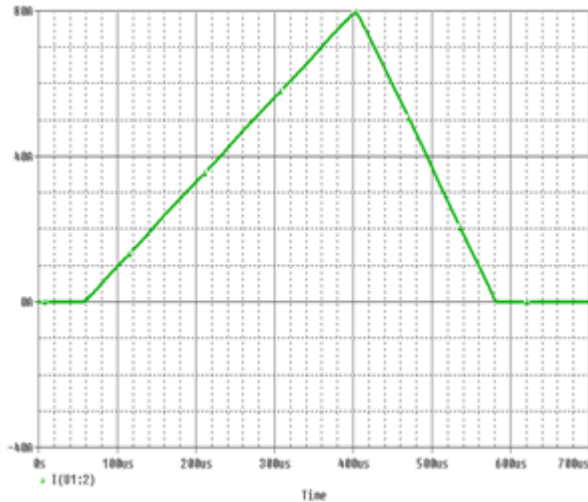

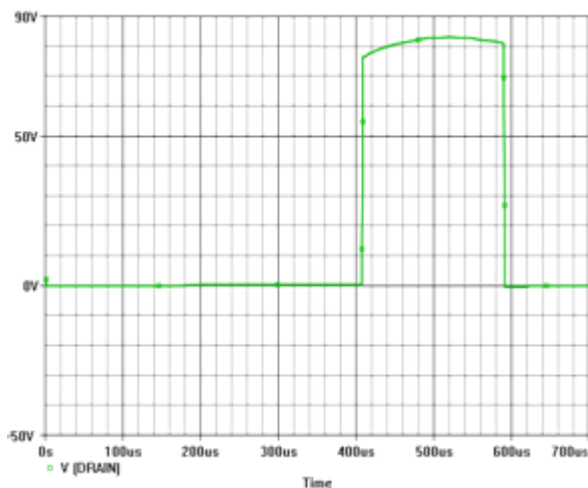**Figure 9a.** imulated drain current for the VDMOSFET transistor

Figure 9b. Simulated drain Voltage (V_{DS}) for the VDMOSFET transistor with self heating effect
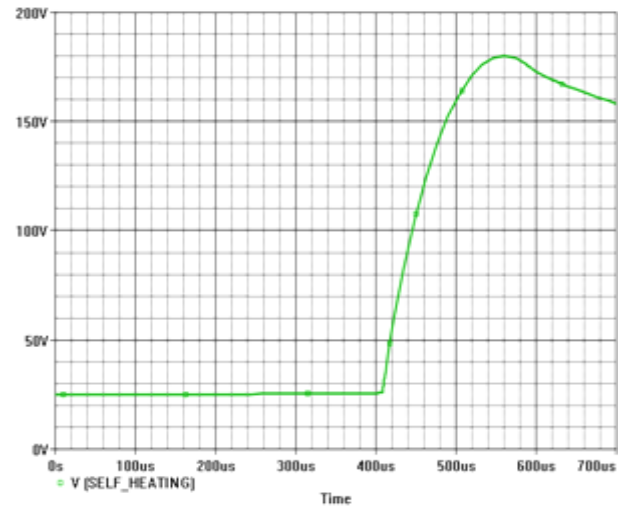

Figure 9c. Simulated Junction temperature ($V_{SELF-HEATING}$) for VDMOSFET transistor
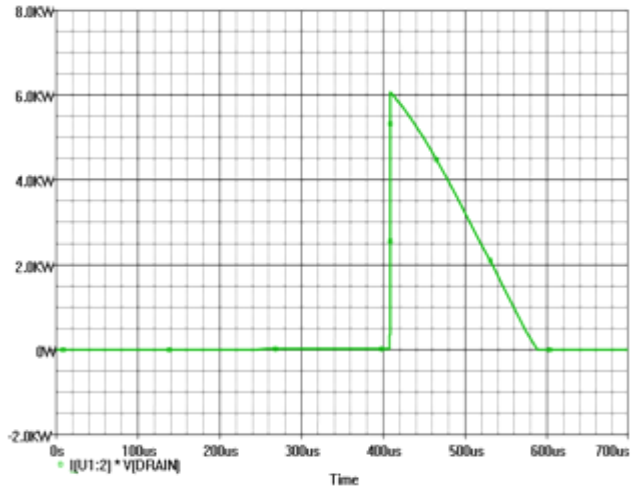

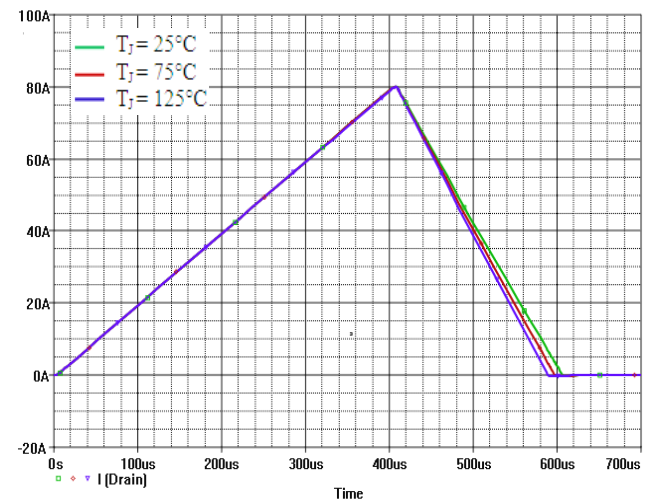**Figure 9d.** Simulated power loss ($V_{DS} \cdot I_{DS}$) of the VDMOSFET self-heating model

Figure 10a. Simulated drain current (I_{Drain}) at 25℃, 75℃ and 175℃ of VDMOSFET self-heating model
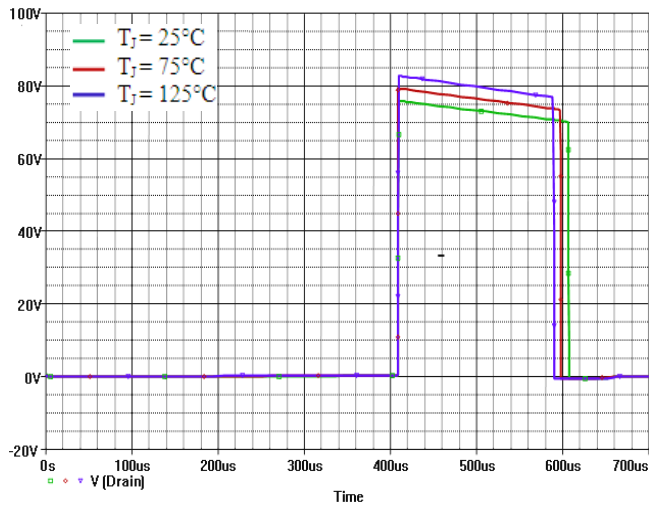
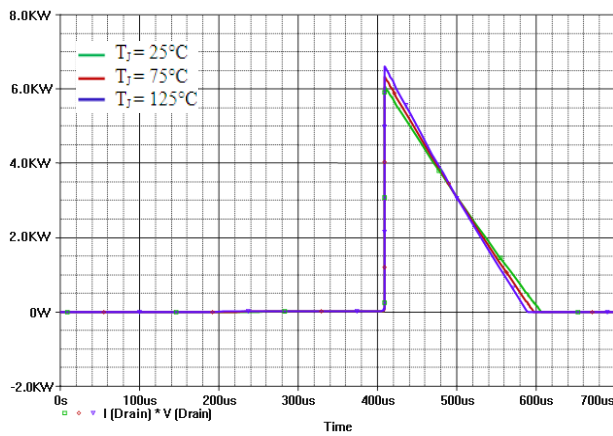**Figure 10b.**   Simulated drain voltage (V_Drain) at 25 ℃, 75 ℃ and 175℃ of VDMOSFET self-heating model

Figure 10c.   Simulated power loss (I_Drain* V_Drain) at 25 ℃, 75℃ and 175 ℃ of VDMOSFET self heating model

6. Junction Temperature Dependency Analysis

Switching behaviour of the VDMOSFET self heating model was tested over junction temperature to show the temperature dependency. Transient comparisons between experiment and simulation were presented at 25℃, 75℃ and 125℃. To observe more clearly the changes associated with temperature, experiment and simulation waveforms are shown in different figures as follows.

7. Simulation Convergence

Many power electronics convergence problems can be solved with two option parameters, Gmin and Rshunt. The Gmin option is available in all PSPICE 9.2 and 10.5 programs. Setting the value of Abstol to 1u will help in the case of circuits that have currents which are larger than several amps. Setting Abstol to a value which is greater than 1u will cause more convergence problems than it will solve. UIS simulations were performed on a Dell Latitude CSx using a

3.8GHz Pentium IV processor with 1GB of memory. Windows XP was the operating system used (virus scan software enabled). PSPICE Schematics version 10.5 was used

Simulation time results were:
- Standard model = 7.9s
- Self-heating model = 13.7s

Simulation time is expected to be longer with the self-heating model due to the dynamic interaction of the junction temperature feedback.

8. Conclusions

An idea of the self heating PSPICE power MOSFET macromodel is described. We have added a simple ladder network model of MOSFET's thermal behaviour. Such a model can be successfully used in most standard electrical circuit simulators for determining semiconductor's operating temperature during various operation cycles domain simulations. In the second part of this paper we examined the unclamped inductive switching behaviour of standard and self heating VDMOSFET model. Good agreement of simulated results confirms the expectations.

REFERENCES

[1]   Z. Bencic Jakopovi, "Identification of Thermal Equivalent-Circuit Parameters for Semiconductors". 2nd IEEE Workshop on Computers in Power Electronics, Bucknell University, USA, 6-7. August 1990., ISBN 0-87942-572-1, pp. 251–260

[2]   Z. Chen, D. Boroyevich, R. Burgos, F. Wang, "Characterization and modeling of 1.2 kV, 20 A SiC MOSFETs," IEEE Energy Conversion Congress and Exposition (ECCE), 20-24 Sept. 2009, pp. 1480-1487.

[3]   N. Phankong, T. Funaki, T. Hikihara, "A static and dynamic model for a silicon carbide power MOSFET," 13th European Conference on Power Electronics and Application, 8-10 Sept. 2009, pp. 1-10.

[4]   K. Sheng, L. C. Yu, J. Zhang, and J. H. Zhao, "High temperature characterization of SiC BJTs for power switching applications," Solid State Electron., vol. 50, no. 6, pp. 1073–1079, Jun. 2006.

[5]   F. Di Giovanni, G. Bazzano, A. Grimaldi,"A New PSPICE Power MOSFET Subcircuit with Associated Thermal Model", PCIM 2008 Europe, pp. 271-276.

[6]   T. Funaki, N. Phankong, T. Kimoto, T. Hikihara, "Measuring terminal capacitance and its voltage dependency for high-voltage power devices," IEEE Transactions on Power Electronics, vol. 24, no. 6, pp.1486-1493, June, 2009.

[7]   D. T. Zweidinger, S. G. Lee, R. M. Fox, "Compact Modeling of BJT Self-Heating in SPICE", IEEE Transactions on Computer-Aided Design of IC and Systems, Vol. 12 No. 9, pp.1368-1375, 1993.

[8]   K. Sheng, L. C. Yu, J. Zhang, and J. H. Zhao, "Maximum

Junction Temperatures of SiC Power Devices'' IEEE trans-actions on electron devices, vol. 56, no. 2, february 2009

[9] A. Hefner, "Simulating the dynamic electrothermal behaviour of power electronic circuits and systems", IEEE Transactions on Power Electronics, V0l.8, No.4, Oct. 1993.

[10] P. Nance, M. Marz, Thermal Modelling of Power Electronic System. PCIM Europe, 2/2000, pp. 20–27.

[11] A. Maxim, D. Andreu, J. Boucher, "SPICE electrothermal modeling of power integrated circuits", IEEE MIEL'97 Conf

[12] Apendoorn, S. Schmitt, H.W. DE Donker, "An electrical model of a NPT-IGBT including transient temperature effects realized with PSPICE Device Equations modeling", Proceeding of IEEE ISIE'97 Conference, pp. 223-228.

[13] A. Maxim, D. Andreu, J. Boucher, "SPICE electrothermal

modeling of power integrated circuits", IEEE MIEL'97 Conference, pp. 479-482, 1997

[14] Q. Chen, X. Yang, Z. Wang, L. Zhang, and M. Zheng, "Thermal design considerations for integrated power electronics modules based on temperature distribution cases study," in IEEE PESC Rec., Orlando, FL, Jun. 17–21, 2007, pp. 1029–1035.

[15] S. Sze, "Physics of Semiconductor Devices", New York. Wiley, 1981

[16] T. Tsividis, "Operation and Modeling of the MOS Transistors", New York, Mc Graw-Hill, 1987

[17] Fischer K, Shenai K. Electrothermal effects during unclam-pedinductive switching (UIS) of power MOSFET's. IEEE Trans Electron Devices 1997;44(5):874–8.