Microelectronics and Solid State Electronics 2012, 1(2): 47-52
DOI: 10.5923/j.msse.20120102.05

Ultra-Low-Power Ultra-Fast Hybrid CNEMS-CMOS FPGA

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Abstract Static power consumption has become a major concern in the design. To address this, we have designed a novel Nano-Electro-Mechanical (NEM) switch with virtually zero leakage current, 1 to 2 Volts operation voltage, 1 ns switching time, > 1 GHz fundamental resonant frequency, and nanometer-scale footprint. Positive and negative channel switches from Complementary NEMS (CNEMS), similar to CMOS. Due to compatibility between CNEMS and CMOS, these CNEMS switches can be hybridized with CMOS at the metallization or device. In this paper, we present the CNEMS design, its electrical properties and a hybrid FPGA with CNEM switches. We used VPR to simulate the MCNC benchmark circuits routed on our hybrid FPGA for power and delay. Our experimental results show an average 98%, 85%, 71% and 99.99% reduction in critical path delay, routing energy, total energy, leakage power when comparisons are made with FPGA design using pure CMOS technology (180 nm technology and hybrid CNEMS and 180 nm CMOS).

Keywords FPGA, HYBRID CNEM-CMOS, NEMS

1. Introduction

CMOS integrated circuit technology provided a continuous improvement in integration level, cost and performance over the last four decades. This has lead to tremendous development in computation, data storage and information processing. Energy and power dissipation for the sub-nanometer CMOS increased drastically due to short channel effect, sub-threshold leakage, hot carriers injection, intra-die, inter-die process and thermal variations. Energy and power are more important for FPGA designs which are constrained by higher power consumption when compared to Application Specific Integrated Circuits (ASIC). This limits the use of FPGA. It was observed that in FPGA, programmable interconnection[9], and resources consume significant energy at the cost of offering flexibility[8] to the design.

Significant amount of research work has been attributed to designing energy efficient FPGA architecture and routing efficient algorithms. In[6, 10], they realized power efficient FPGA by assigning programmable low VDD (0.9V) to non timing critical CLB's and high VDD (1.1V) to the timing critical CLB. They reported an average power saving of 61% at the cost of increased area. The increased area is due to the use of additional level converters and routing multiplexers.

In[13], they proposed a new FPGA routing switch that can be programmed to operate in three modes: high-speed, low-power or sleep-mode. In the sleep mode, applied to unused switches, offers significant leakage reductions. In the sleep-mode the leakage power is reduced by 36%-40% over the high speed mode, and the dynamic power is reduced by up to 28%.

[14] Proposed reducing FPGA power by the use of Dual threshold CMOS (DTCMOS) based switches instead of NMOS. The area overhead is kept to minimum. The sleep transistor is used to reduce the sub-threshold voltage. They reduce the power-delay product by 16% and by of 20% in active and standby mode, respectively.

In[16], The NEMS switch[18] is proposed to be used in NEMS-CMOS hybrid LUT, and it is compare to CMOS LUT in terms of power and delay. The simulation results show that the delay is almost the same, but the power is reduced by 90% in the NEMS-CMOS LUT over CMOS LUT.

In[17], CMOS-Nanorelay FPGA (cFPGA) was developed using new two CMOS transistors and one NEMS relay. They proposed using vertical carbon Nanotube which is relatively easier than horizontal carbon Nanotube to fabricate. This results in reducing dynamic power by 30%. Carbon nano-tubes are much harder to make and cannot integrate seamlessly with current CMOS technology.

In this paper, we introduce a configurable Complimentary Nano-Electro-Mechanical Switch (CNEMS) metallic switch

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Published online at http://journal.sapub.org/msse

ing device as a replacement of CMOS devices in the switch and connection block components found in FPGA architectures. The new metallic CNEMS switch uses the same CMOS fabrication steps and materials. This makes it easy for the CNEMS switch to be "dropped" in and hybridized, seamlessly, with CMOS at the metallization or at the device level to manage leakage current and power consumption. The CNEMS with its innovative structure operates at 1GHZ resonating speed, has a low turn on voltage between 1 to 2 volts, near zero current leakage, and near zero parasitic capacitance. The CNEMS switch significantly reduces the power consumption, increases the FPGA speed and offers seamless integration with CMOS technologies.

The rest of this paper is organized as follows: Section 2 describes the CNEMS device structure. Section 3 presents the 3D FEA physical device model, illustrates extraction of mechanical and electrical properties and explains CNEMS digital logic gates. Section 4 explores the approach and presents experimental setup and results. Conclusions are presented in section 5.

2. Device Design

Figure 1 shows structure of a four terminal NEM switch. The switch has a moveable cantilever beam with nickel coated on an oxide layer. In initial position, the direct metal-metal contact between drain/source and cantilever form direct current path. With applied voltage V_{gb} between gate and cantilever, the electric force and the small Van der Waals force attract the cantilever to move towards the gate. During the attraction, a gap between the cantilever and the gate decreases. With the voltage reaching a threshold value or pull-in voltage (V_{pi}), the gap reduces to a critical value, 1/3 of initial gap and then the cantilever abruptly contacts the gate to break the direct current path between drain and source. When the voltage V_{gb} between the gate and the cantilever decreases to a small value or pull-out voltage (V_{po}), the cantilever leaves the gate and contact drain and source to form the direct current path again.

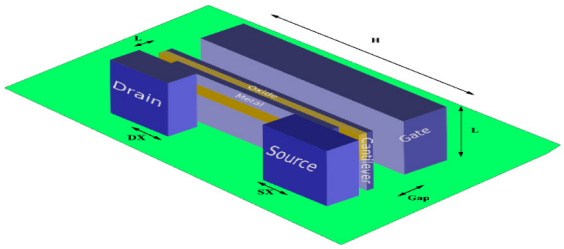
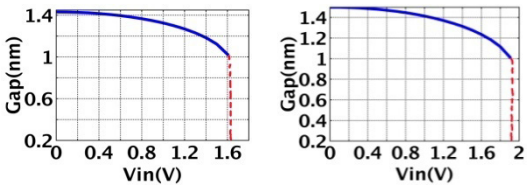


Figure 1. Schematic of a four terminal switch geometry



(a) (b)

Figure 2. (a) Pull-in voltage with Van der Waals force 1.64 V. (b) Pull-in voltage without Van der Waals force 1.95 V

3. Physical Device Model and CNEMS Digital Design

A. Physical Device Characteristics

To capture multi-physics phenomena of a four terminal switch, a 3D FEA physical device model is constructed using FEA simulation tool (COMSOL multi-physics). This model is capable of capturing the multi-physics of the four terminal NEM switch as well as re-producing its electro-mechanical characteristics.

Pull-in voltage: The pull-in voltage is solved by static-parametric solver in COMSOL multi-physics. In the solver, the fringing effect is ignored as a result of the small gap (1.5 nm)[20]. We consider Van der Waals[21] force on the cantilever surface facing to the gate due to the small gap (1.5 nm). The attractive Van der Waals force reduces the pull-in voltage about 0.3 V. The simulated pull-in voltages with Van der Waals force and without Van der Waals force are shown in Figure 2. Note, the simulation stops just before the contact happens.

Switching time: The time dependent solver in COMSOL multi-physics is used to solve switching time with applying pull-in voltage between the cantilever and the gate. The simulation result in Figure 3(a) shows the switching time is about 1 ns. The input capacitance is a very important parameter for the switch. The change of the capacitance with time shown in Figure 3(b) is modelled by setting capacitance density on the cantilever surface. The boundary integration function integrates the capacitance between the cantilever and the gate for each time point.

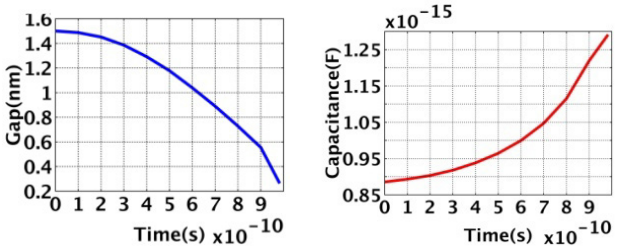


Figure 3. Switching time versus the gap between the cantilever and the gate and gate capacitance versus the time

B. CNEMS Digital Design

The basic NEMS switch is shown is Figure 4. The switch consists of three fixed terminals and one moving cantilever. These are the Source(S), the Drain (D), the Gate (G), and the moving metallic cantilever Body (B). The body B and both S and D are connected while the gap between G and B is 1.5nm. If the voltage potential difference between G and B (V_{gb}) is less than the pull-in Voltage (V_{pi}), then switch is in the *ON*-state. In the *ON*-state, B connects both S and D and provides a metallic low resistance connection between S and D. Our switches are fabricated using Nickel which has large Young's modulus, the ability to withstand high switching cycle and the switch contact resistance between the channel and the S/D is around 90 Ω.

If $V_{gb} > V_{pi}$, then the electrostatic and a small inter molecular force (Van der Waals) cause a displacement in the

cantilever body (B) that disconnects S from D causing the current from S to D I_{ds} to be limited to a near zero leakage current. In this case, the switch is in the *OFF*-state. When the switch is in the *OFF*-state, the spring restoring force of the movable cantilever beams always overcome the Van Der Waals force when gate voltage is sufficiently below V_{po} (pull-out voltage).

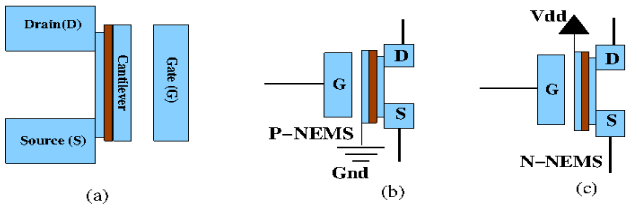


Figure 4. (a) NEMS device structure; (b) P-NEMS device configuration; (c) N-NEMS device configuration

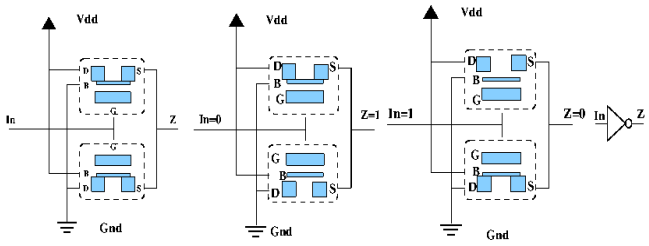


Figure 5. CNEMS inverter

Logically, the NEMS and the CMOS switches operate similarly. Thus, the design and implementation of a digital circuit using the NEMS switches are fundamentally similar to the process of designing a circuit in CMOS. Similar to an MOS device, the NEMS switch consists of three terminals the source (S), the gate (G) and the Drain (D) as shown in Figure 5. Depending on the voltage differential between the G and B terminals, the switch can be '*ON*' (D is connected to S) or '*OFF*' (S is not connected to D).

The inverter consists of two NEMS in series, one PNEMS and one NNEMS shown in Figure 5. When the input voltage In = 0, the differential voltage between G and B of the PNEMS is zero and in this case this device turns '*ON*'. The differential voltage between G and B for the NNEMS is different from zero and this device turns '*OFF*'. Thus the output voltage at Z is VDD or logic 1. When In = 1, the PNEMS turns '*OFF*' and the NNEMS turns '*ON*', the output voltage Z is equal to logic 0. CNEMS NAND and NOR gates can be constructed in the same way.

4. Power Reduction in CNEMS-CMOS FPGA

A. FPGA Background

Figure 6(a) shows a typical island style 2-D Field Programmable Gate Array (FPGA). This FPGA is composed of an array of Configurable Logic Blocks (CLBs), a programmable interconnection switch box and I/O Pads. The CLBs store the truth tables of functions in Random Access Memory (RAM). The switch box is implemented using CMOS programmable switches as shown in Figure 6(b). In this configuration the CMOS switch current leakage and capacitive/resistive causes the FPGA to consume more power and to operate at a lower clock frequency. In this paper, we introduce a novel Nano-Electro-Mechanical Switch (NEMS) configurable architecture which can be used to replace the CMOS switches in the FPGA switch box (Figure 6(c)). Unlike CMOS switches, the NEMS switch operates with a near zero off-state current leakage and a very low on-state resistance (30Ω). The reduction in the off -state current leakage and the very low on-state resistive loading allow the FPGA to operate at lower power and faster clock rate. The NEMS switch in this environment is used only during configuration. This use of the NEMS switch overcomes the speed degradation caused by the mechanical movement. The configuration time may increase slightly by it is compensated with the speed and power dissipation reduction during computation cycles. We study island style FPGA architectures for our work and we use the terminology adopted in[15].

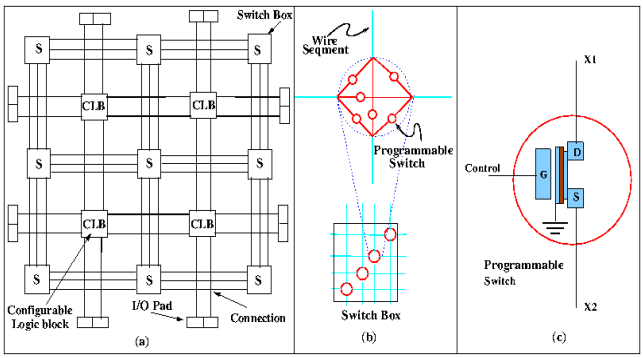


Figure 6. FPGA architecture; (a) Island-style FPGA consisting of I/O Pads, Configurable Logic Block (CLB), and Switch Blocks for routing; (b) Switch Box architecture design and programmable switches; (c) A Programmable NEMS switch. When Control=0 then X1and X2 are connected and not when Control=1

B. Experimental Setup and Results

To illustrate energy efficiency of hybrid CNEMS-CMOS FPGA comparing baseline CMOS FPGA, we performed evaluation on them at spice level (low level) and architectural level (high level). Tristate buffers used in routing switches of hybrid CNEMS-CMOS FPGA are designed using CNEMS which are SRAM-free and offer order of magnitude low resistance. The experiment is divided into two parts. Part I compares power and delay results obtained from low level analysis using spice and high level analysis performed using VPR 5.0 framework[15]. Spice simulations provide base framework to evaluate hybrid FPGA vis-à-vis CMOS FPGA and establishes the accuracy of results obtained by VPR. Part II evaluates MCNC benchmark circuits on hybrid FPGA and CMOS FPGA using VPR 5.0 framework.

We developed a spice model of CMOS FPGA framework with K (LUT size) = 4, N (Number of logic blocks in a CLB). Power and delay analysis is carried out in each instance for varying number of logic blocks in FPGA using ELDO spice

and 180 nm technology. For hybrid architectures, an equivalent spice level description of CNEMS switch block is derived and simulated using *NemSim*[22].

VPR framework which has integrated power model[19] is used in our analysis. This power model is based on transition density and static probability of a signal to compute the dynamic power. Short circuit power is calculated as a percentage of dynamic power which is one of the parameter in architecture file. Input signal probability is assumed to be 0.5 and transition probability of 0.5. VPR analysis is based on values supplied through architecture files which make it flexible for usage across FPGAs with varying LUT sizes (K) and CLB sizes (N), switch block and connection block designs. In our work, we modified the power model to account for the CNEMS characteristics. More specifically we introduced switch parameters (Resistance (R=95Ω,C_{in}=8.4e-16, Cout=0) in the architecture files to take the effect of CNEMS usage. Leakage power and switch block power calculations are modified accordingly in the power model to characterize CNEMS power dissipation.

The power and delay measurements using spice are compared VPR observations in which number of logic blocks present in FPGA is varied from 1 through 4. VPR results show great correspondence with spice. This helps in asserting the fact that VPR level evaluation of hybrid FPGA stands with good accuracy and provides a strong motivation for evaluation of complex benchmark circuits using VPR.

We used CNEMS which has 1V operating voltage with 1e-10 leakage current for these comparisons. We observed on an average 75% decrease in total power and 97% reduction in critical path delay with the use of hybrid FPGAs. These observations provide us with prima facie understanding about the impact of using CNEMS switches in FPGAs and the accuracy of their evaluation using VPR. TSMC 0.18nm technology has been used for this study.

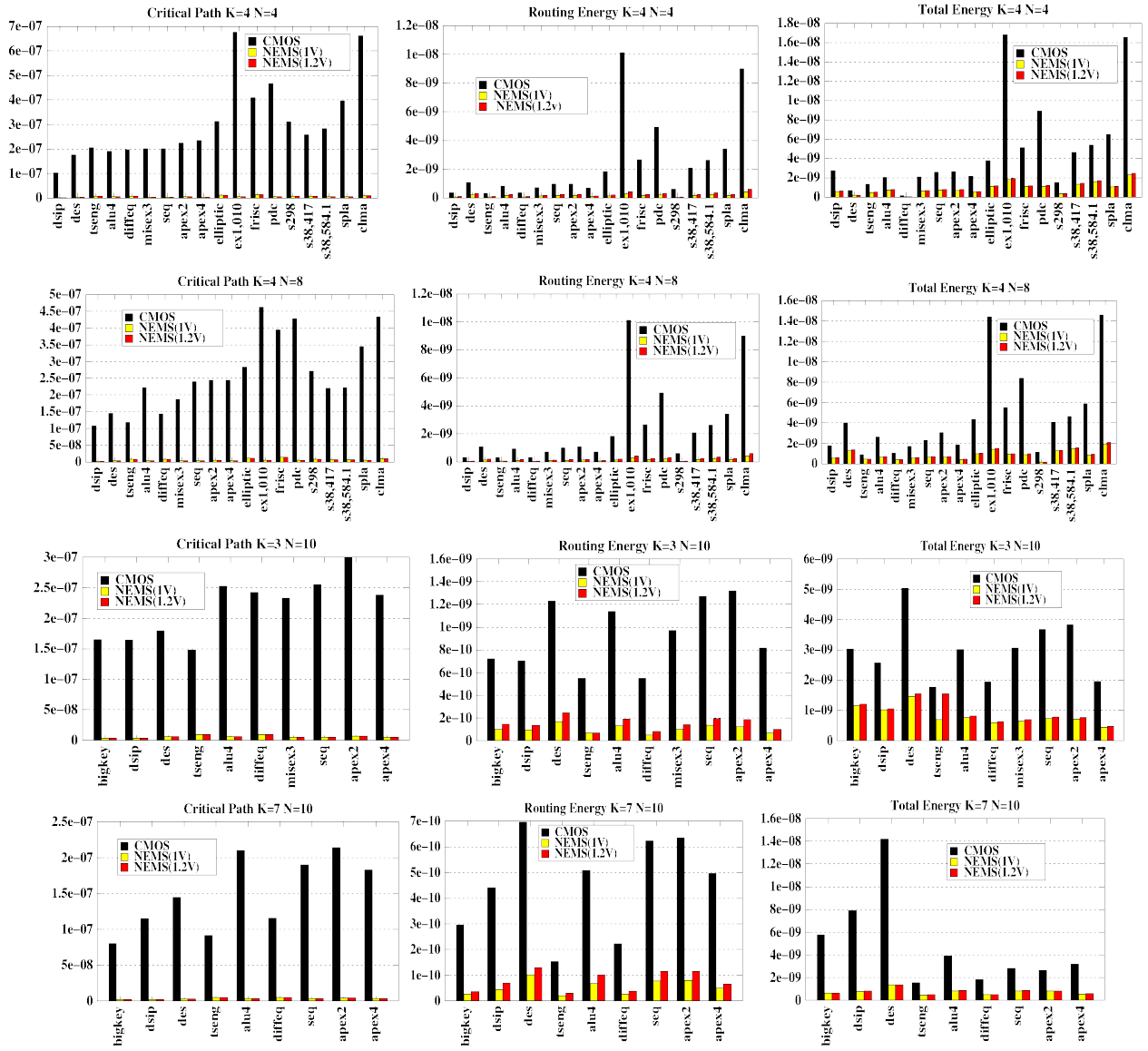


Figure 7. Critical path saving, routing energy saving and total energy saving of different MCNC circuits for K=4 and N=4, K=4 and N=8, K=3 and N=10 and K=7 and N=10 settings

To demonstrate the efficiency of proposed hybrid architectures, a detailed performance evaluation and comparative study are carried out vis-à-vis CMOS FPGA on top MCNC benchmark circuits. We used the modified VPR power model and architecture files, used in part I to perform these experiments. In this work, we used two CNEM switches with operating voltages of 1V and 1.2V and leakage currents of 1e-10 and 1e-16 respectively. CNEMS switch blocks in FPGA design primarily impacts the routing energy consumption and critical path delay. Hence we reported routing energy, leakage power and critical path savings obtained for a combination of LUT sizes (K) and Cluster Sizes (N) - 4,4, 4,8, 3,10 and 7,10.

Figure 7 shows savings in routing energy, total energy, leakage power and critical path delay. It was observed that on an average critical path delay reduced by 97.55%, routing energy by 85%, total energy by 71% and more predominantly leakage power by 99.9%. Significant reduction in energy can be attributed to the fact that CNEMS has zero leakage in the OFF state. It was also observed that Critical Path delay is reduced primarily because Tdel of CNEMS switch is considered zero as there exists no prorogation delay through CNEMS once configured. It can be thought of as a metallic contact when configured. Output Capacitance (Cout) of CNEMS is zero as there exists no parasitic capacitance between Source, Drain and Body. With the nature of results obtained when compared with CMOS, it can be affirmed that CNEMS has a tremendous impact in designing energy efficient FPGA.

5. Conclusions

In this paper, we presented a configurable CNEM metallic switching device as a replacement of CMOS devices in the switch and connection block components found in FPGA architectures. The new metallic CNEM switch uses the same CMOS fabrication steps and materials, operates at 1GHZ resonating speed, has a low turn on voltage between 1 and 2 volts, near zero current leakage, and near zero parasitic capacitance. We showed, experimentally, that the CNEM switch significantly reduced the power consumption, increased the FPGA speed and offers seamless integration with CMOS technologies. In our experiment, the CNEM FPGA architecture achieves an average 98%, 85%, 71%, and 99.99% reduction in critical path delay, routing energy, total energy, leakage power over CMOS (180nm) FPGA architecture.

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