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Envelope Tracking Line-up Design Considerations with High Efficiency Linearizable Inverse Class-F Driver Amplifier

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Abstract In this paper, comprehensive design considerations for multi-stage envelope tracking power amplifier line-up design with a 10W GaN HEMT switch mode driver amplifierwas presented to realized optimum overall power added efficiency.Crest factor reduction algorithm and non-linear switch mode driver design for efficiency and linearization were studied. Also, a high efficiency inverse class-F amplifier was implemented with efficiency as 44.8% for LTE 20MHz signaland characterized to provethe concept of applying linearizable inverse class-F amplifierenvelope tracking driver purpose.

Keywords Crest factor Reduction, Efficiency,Envelope Tracking, GaN HEMT,Inverse Class-F,Line-up, Power Amplifier, Switch Mode

1. Introduction

In wireless communication infrastructure industry, to enhanceradio power amplifier (PA) efficiency, one of thepromising techniques is envelope tracking (ET). Principally, PA supply is varied based on the monitored envelope levelsand changing all the timeso as to right meet the output power level of PA at a certain moment of time to achieve high efficiency.

With current high efficiency transistor technology such as GaN HEMT switch mode PA, final stage or single stage cannot achieve sufficiently high gain to keep the radio transistor line-up high efficiency. Lining up envelope tracking on both driver amplifiers and final stage is capable to boost overall or cascaded power added efficiency (PAE). Consequently, line-up envelope tracking can provide more improvement in radio efficiency, resulting in more profitable in a wireless system by cutting overall costs to operate the system, especially for high output power base stations.

However, although it is highly desired to enhance the efficiency of driver amplifier by ET, choosing correct high efficiency PA topology with proper characterizations and considerations is critical to make a well matching between ET driver and final stage to maximize the performance of line-up.

This paper mainly focuses on ET switch mode driver amplifier designconsiderations for system line-up, analysis and inverse class-F amplifier characterization for ET performance optimizations. Thenecessity of ET line-up for cascaded PAE was analysedmathematically in section II. In section III, the basic wide band supply modulator character was illustrated. A pieceof LTE 64QAM 20MHz signal source with featured clipping was used in this paper as stimulus for analysis. The relationship between ET and clipped signal probability density function (PDF), instantaneous peak error vector magnitude (EVM) were discussed in section IV. In section V, with regard of inverse class-F topology, a 10W switch mode driver amplifier was designed and characterized based on GaN HEMT technology. Linearization capability of this kind of high efficiency driver was studied as well. Finally, conclusions were given in section VI.

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2. Power-Added Efficiency& ET PA Line-Up

Power-added efficiency (PAE) is an important metric for ET PA efficiency in that it is not only a measure of efficiency, but also taking all of the power input into consideration, which means for the ET PAs producing the same output power, the ones with higher PAE will ultimately work for a longer time if the same amount of energy was provided.

However, in ET PA working scenarios, it operates in the compression region over most of envelopes, usually being pushed seriously into saturation in short instants, resultingin gain loss for final stage, which finally reduces the PAE of ET PA to some extent. According to the below analysis in Fig.2

and gain character of commercial GaN HEMT transistors, the gain threshold is set at about 10dB for ET PAs,below which overall efficiency, orPAE, will start to degradeseriously. Therefore, ET PA line-up is taken into account bysharing one modulator to further increase PAE of an ET PA design, as shown in Fig.1.

The drain or collector efficiency of PA is defined as

$$\eta = \frac{P_{out}}{P_{DC}} \times 100\% \tag{1}$$

Also, the PAE is defined as equation (2), which PAE can be

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\% = \eta \times \left(1 - \frac{1}{G}\right) \times 100\% \tag{2}$$

interpreted as the efficiency to convert the DC supply power into the output RF power which is remained over after the direct contribution from the input RF power has been removed. It can also be rearranged in terms of drain efficiency and RF power gain, as shown in the 3D plot of Fig.2.

With regard of PA line-up in Fig.1, the line-up PAE equation can be deduced as below,

$$PAE_{Line-Up} = \frac{P_{out2} - P_{in1}}{P_{DC1} + P_{DC2}} \times 100\% = \frac{G_1 \cdot G_2 - 1}{\frac{G_1}{\eta_1} + \frac{G_1 \cdot G_2}{\eta_2}} \times 100\% \tag{3}$$

According to the final stage design in lab, the typical value of ET PA final stage can be assumed as constants, G_2 =10.5dB=11.22, η_2 =62%=0.62 for the final stage. Therefore, the contribution of efficiency and gain of driver amplifier to ET PA line up was plotted in Fig.3.

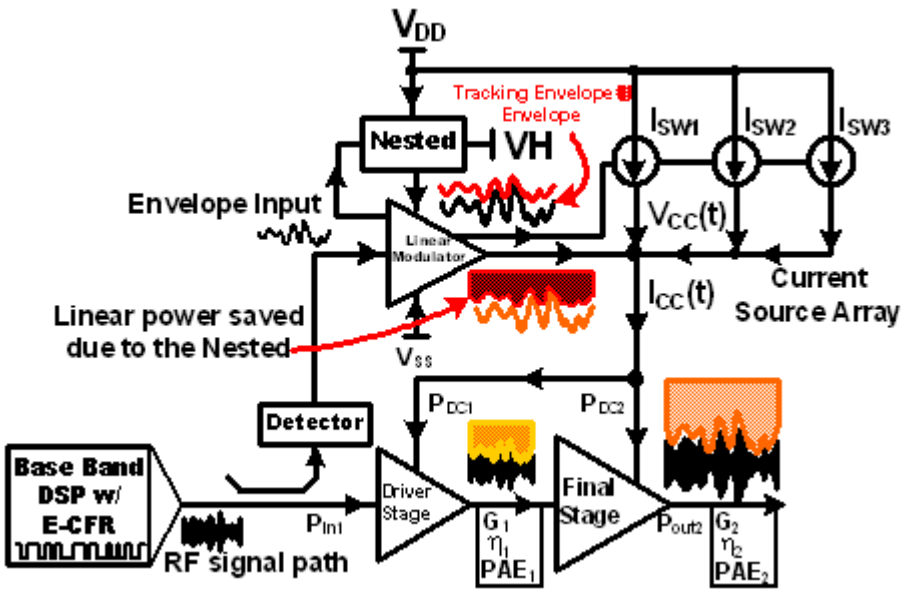

Figure 1. ET PA line-up block diagram including modulator schematic

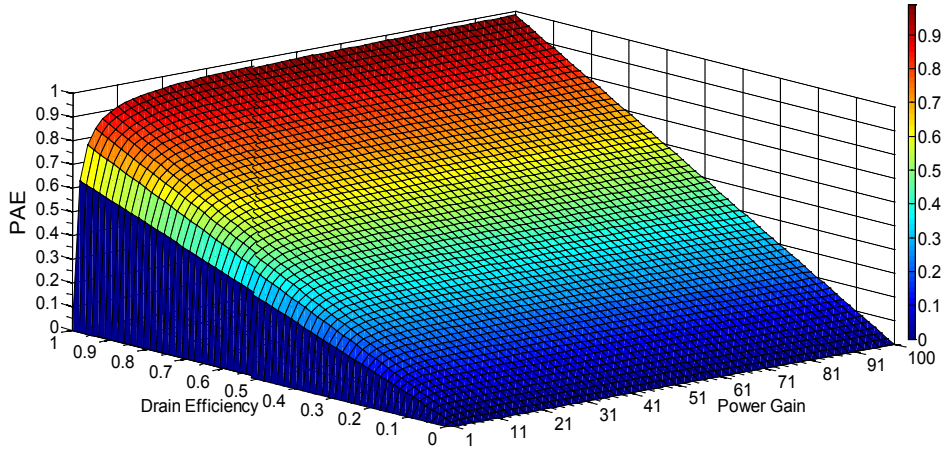

Figure 2. PAE character plot vs. power gain and drain efficiency

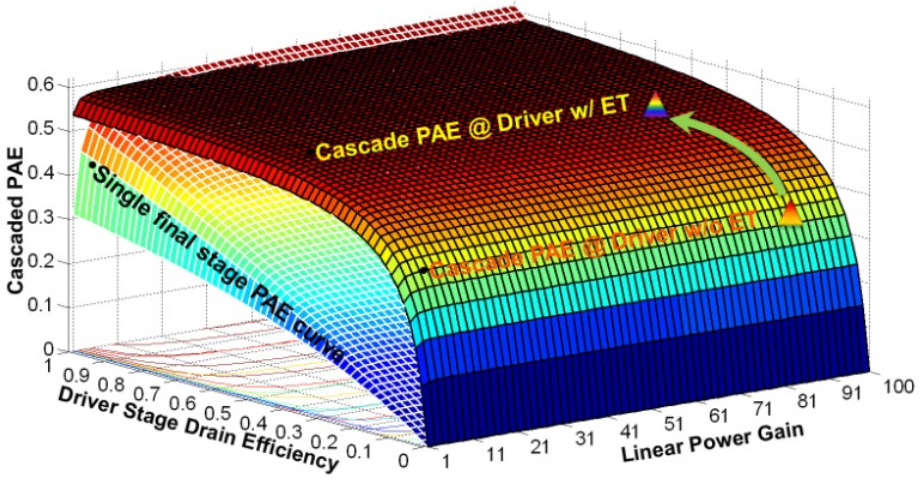

Figure 3. Line-up cascaded PAE character vs. driver amplifier power gain and its drain efficiency compared to a single stage PA

In high power gains scenarios, for single final stage PAE in Fig.3, there is a quasi-linear relationship between PAE and its drain efficiency, where PAE would drop dramatically if ET drain efficiency dropped. However, if a two-stage line-up was applied, that relationship would be transformed into almost a constant between line-up PAE and its drain efficiency in Fig.3, which means line-up PAE would keep high and tolerate more drain efficiency degradations. Also, due to the line-up gain increase, there is a minor PAE drop for a low gain final stage case when a line-up was applied, compared to a single stage ET PA, as shown in Fig.3.

In conclusion, line-up configuration for high efficiency ET PA is essential for practical applications and ET driver amplifier deserve more sophisticated design considerations.

3. Wideband Supply Modulator

The architecture of supply modulator in this paper was illustrated in [2]. The modulator bandwidth requirement is challenging due to the character of envelope spectrum. Although the envelope signal power of LTE takes the lo in share of power, about 96%, within its RF signal bandwidth from DC, e.g. 100MHz LTE-Advanced envelope spectrum shown in Fig.4, the modulator bandwidth should be designed with five times of RF bandwidth, considering both amplitude and phase spectrum shape of envelope.

However, switching supply fails to provide high efficiency for such a high speed, the switching loss is tremendous. Therefore, linear modulator part needs to boost efficiency for wider bandwidth applications, which can be implemented by the proposed nested structure by adding an additional peak efficiency point into linear part modulator [2], as shown in Fig.5.

In Fig.5, the green and blue simulation results are the instantaneous efficiency of linear part with nested voltage ratio α =2/3 & 1/2 respectively, trying to fit envelope voltage PDF of LTE 20MHz 64QAM signal with the other peak efficiency point, boosting the efficiency of the wide band linear modulator.

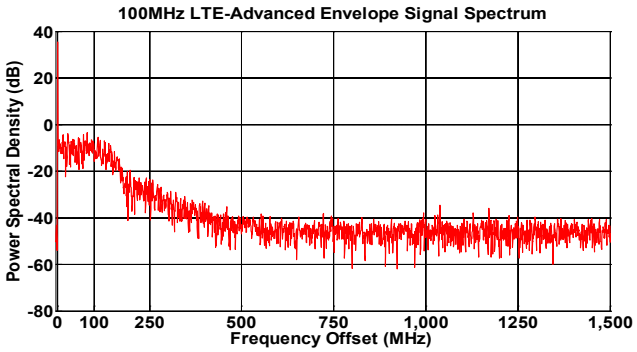

Figure 4. In LTE-Advanced with 100MHz signal bandwidth, in-band 100MHz bandwidth takes up 96% power of the envelope signal

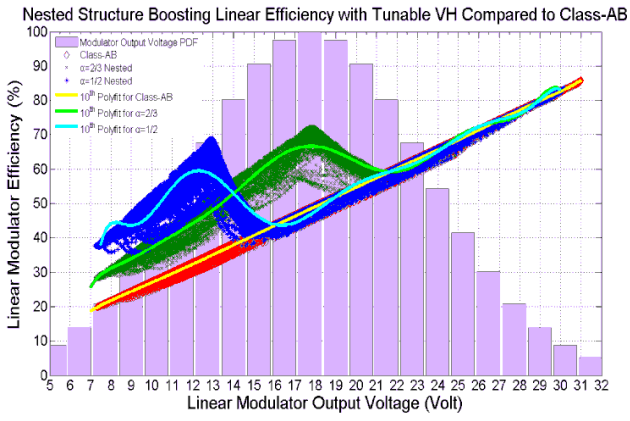

Figure 5. Nestedstructureefficiency boosting simulation results with a LTE 20MHz 64QAM compared to Class-AB linear part

Similarly to LTE-A 100MHz scenario, it requires at least 100MHz modulator bandwidth for 20MHz LTE signal to keep less distorted. Thus, the modulator in this paper was tuned with 131.5MHz bandwidth in Fig.6, tested with 50 Ohm resistive load.

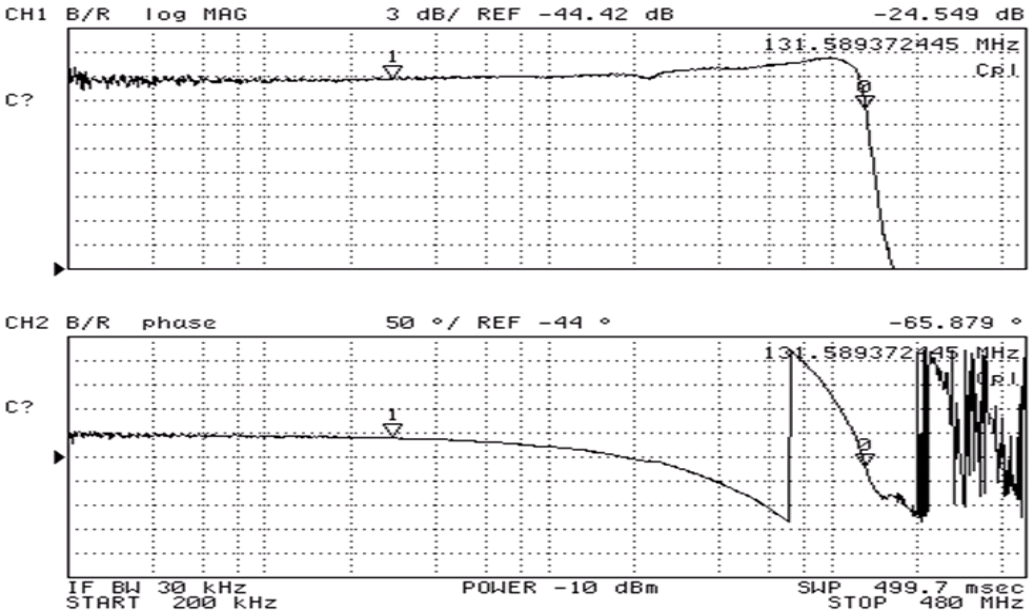

Figure 6. Frequency response measurement results of the modulatorwith a resistive load

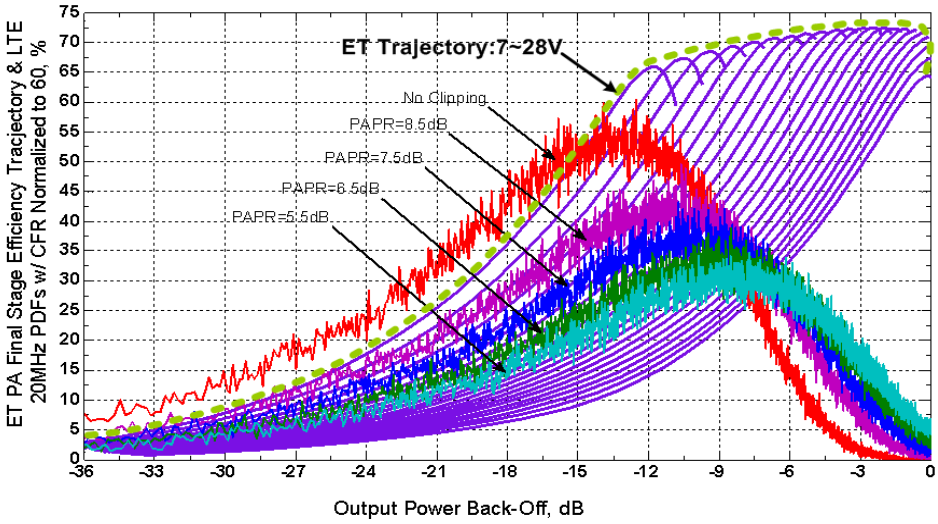

Figure 7. Various clippings of CFR shift the PDF of LTE 20MHz right forward to fit the final ET amplifier stage trajectory

4. Crest Factor Reduction Algorithm for ET

Traditionally, the crest factor reduction (CFR) algorithm contains the crest of modulated signal into PA to make operation possible in higher efficiency region. However, the benefit of CFR algorithm to ET PA efficiency is also obvious.

4.1. CFR Analysis for ET PA

Since the modulation schemes at base band are getting ever more complex, the peak to average power ratio (PAPR) is ever larger and moving toward left side in probability density function (PDF) plot. However, CFR is capable to move it toward right side, avoiding RF PA suffering from too much back-off resulting in average efficiency degradations. Also, in ET scenarios, CFR can make PDF histogram shape more fit for efficiency trajectory of a RF PA transistor with various drain or collector voltages as shown in Fig. 7.

In Fig. 7, ET trajectory was tested and plotted in dashed green by short RF pulse measurement method for the ET PA final stage with supply voltage ranging from 7V to 28V. The maximum CW output power was normalized into 0dBm to easily compare it with different LTE 64QAM 20MHz PAPRs with clipping ranging from 5.5dB to no clipping scenario. About 6dB movement in maximum to the right of the peak probability of PDF was observed. Besides, the probability of occurrence in smaller back-off region has increased significantly. Thereafter, well-clipped modulated signal will fit better into the shape of ET PA trajectory to obtain more efficiency.

In ET PA system, the linear plot of LTE PDF versus supply modulator output voltage could make the effects of clipping to drain or collector modulation more clearly in Fig. 8.

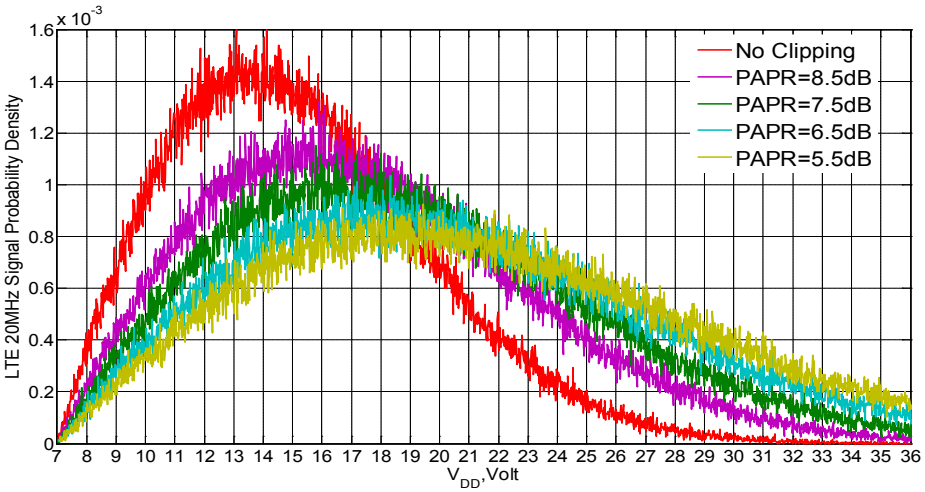

Figure 8. The PDF of LTE 20MHz versus ET modulator output voltage

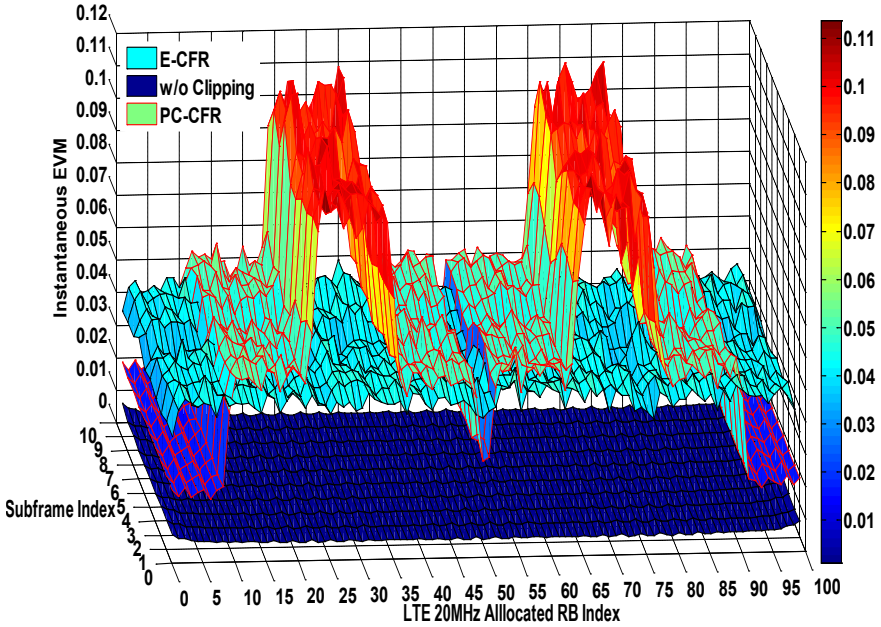

Figure 9. 3D plot of instantaneous EVM vs. allocated RBs and sub-frames in LTE 20MHz to compare performance between PC-CFR and proposed E-CFR

In Fig.8, themodulated signal without clipping will be distributed into low voltage region centred with ~13V. This response of PDF was much narrower than the clipped ones. From the RF transistor perspective, much flatter response of PDF over the operation voltages could provide much better linearity due to the P1dB point moving into high power level dynamically. In other words, the ET PA could provide more efficient power conversion with the same linearity metrics. With considerations of transistor cost, the ET modulator operation with the clipped signal will cover more higher voltages and with more probability, which could draw out more power from the transistor than the lower voltage operation ET PAs, during efficient amplification and make trading off with linearity specifications. Therefore, in the below section, a new CFR optimized from each LTE resource block (RB) was proposed for ET PA performance enhancement.

4.2. The Proposed Equalized CFR for ET PA

There is a trade-off among more crest reduction, spectrum re-growth and error vector magnitude (EVM) degradations. Therefore, CFR algorithms have been studied for the most optimized performance. Peak-Cancellation CFR (PC-CFR) is one of most popular solutions in practical applications. However, it may suffer from serious peak EVM degradations, resulting in lower throughput of base station when clipping is required too hard.

The proposed equalized CFR (E-CFR) algorithm is capable to optimize or equalize instantaneous or peak EVM crossing LTE allocated resource blocks (RBs) and sub-frames, which causes a flat response of EVM overall various with the two axis shown as the 3D plot in Fig.9.

Accordingly, both composite and instantaneous peak EVMs with E-CFR are lower than PC-CFR, resulting in a

much better EVM when clipping is hard as shown in Fig.9 and Table I, e.g. clipped PAPR=6.5dB, EVM under PC-CFR was 5.32%; EVM under E-CFR was 3.21% which is ~ 2% improvement. In the other word, with E-CFR for ET purpose, more clipping can be implemented for better efficiency performance without much degrading modulation quality.

Table 1. Summary of EVM Performance of CFR

PAPR	PC-CFR EVMpk	E-CFR EVMpk	PC-CFR EVM	E-CFR EVM
8.5dB	1.45%	0.89%	1.09%	0.68%
7.5dB	2.98%	1.91%	2.43%	1.62%
6.5dB	6.21%	3.78%	5.32%	3.21%
5.5dB	10.24%	6.38%	8.01%	5.48%

5. Experimental Inverse Class-F Amplifier for ET

To obtain higher efficiency of RF PA for the line-up driver design, one effective way is to utilize harmonic manipulation to realize a switching mode inverse Class-F amplifier. By means of this art, the amplifier has to operate in saturation region and resulting in serious distortions. However, with modern digital pre-distortion (DPD) technology, it could be linearized accepted level to satisfy the specifications by careful and sophisticated design. In this work, an inverse Class-F based on CREE 10W GaN HMET transistor CGH40010 was designed for envelope tracking line-up driver purpose as shown in Fig. 10, which required "friendly" character or optimized memory effect to pre-distortion.

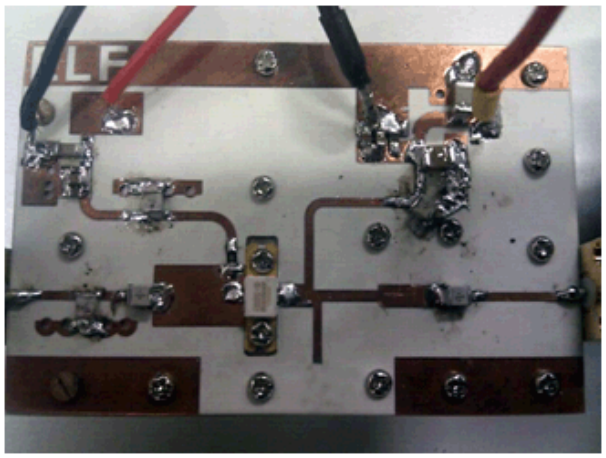

Figure 10. Realized inverse class-F 10W driver amplifier

With the principle of an inverse Class-F RF amplifier, the high efficiency operation was obtained by manipulating limited even and odd harmonics, e.g. only 2nd and 3rd order harmonics of fundamental frequency were considered to generate a quasi-half-sinusoidal voltage waveform and a quasi-square current waveform at the transistor output. In practical design, compensation transmission lines for the parasitic of bonding wire inductance in series and package plane were considered. The micro stripcompensation and matching network design was verified by simulations in package plane. The required loading condition was implemented by control of the device non-linear output capacitance and parasitic inductance. The simulated inverse class-F instantaneous voltage and current waveforms with the harmonic terminations were as shown in Fig. 11 below. The phase difference between voltage and current was approaching to zero, realizing high efficiency on the resistive fundamental load impedance.

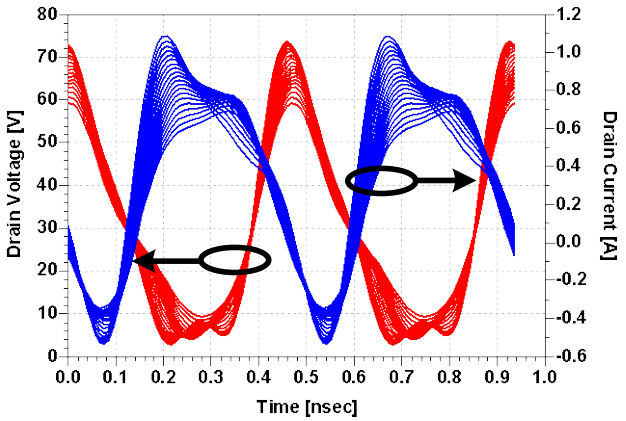

Figure 11. Simulated inverse class-F instantaneous waveforms at package plane of a 10W GaN HEMT transistor

From Fig. 12, the dynamic load lines of the proposed inverse class-F were illustrated. Due to the optimization work, the load lines were unlike traditional inverse class-F with "looping character". However, it was like a"twist looping" character to provide better peaking and sinking effects by utilizing compensation of the internal parasitic in package and manipulations of the asymmetric current waveform engineering , which further reduced the power loss.

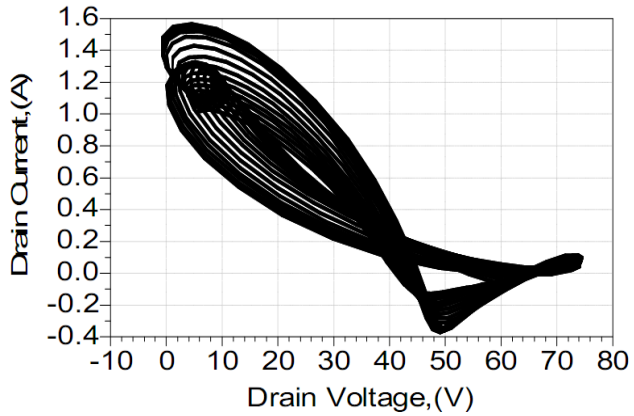

Figure 12. Simulated inverse class-F load lines at package plane of a 10W GaN HEMT transistor

By the means of tuning the fundamental and harmonic load impedance up to the third order, a linearizable and high efficiency inverse class-F driver amplifier has been measured at a fundamental centre frequency of 2.14GHz. The power sweep experiment was implemented with LabVIEW automatic test platform in lab, the record data was plotted as shown in Fig.13, compared to the simulation data

with the same conditions.

From Fig.13, the experimental results showed good consistency with the simulation results, which proved the accuracy of large signal GaN HEMT models provided. A peak drain efficiency of 76.6% has been measured with 40dBm device output power and approximately 5dB of gain compression. Furthermore, the peak PAE point happened with approximately 4dB gain compression with 74.4%.

Also, a frequency sweep with fixed input power 25dBm has been implemented to observe the bandwidth of the design as shown in Fig. 14 as below.

When looking at the device output bandwidth performance, the measure drain efficiency was still above 60%, ranging from 2070MHz to 2220MHz. Due to the inherent limit of inverse class-F narrow bandwidth, a feature of above 60% drain efficiency over a 7% bandwidth was observed.

It is important to measure the actual specific character for ET driver amplifiers, e.g. ET trajectory, gain compression status at each supply voltage etc. However, traditional fixed supply sweep test method would heat up the RF transistors too much which might not be accurate for ET application due to the different thermal scenarios.

Therefore, short RF pulse amplitude sweep measurement with cooling time intervals was utilized to obtain the true character of transistors under ET.The stimulus was a train of RF pulse sweeping with linearly increasing amplitudes from -5 to 25dBm, accompanying with sufficient cooling intervals. The duration of cooling intervals depends on the duration of pulse length, leaving enough time margins for RF transistor to be cooled down. The supply voltages of each pulse changes from 10V to 30V with an increment equals to 1V. By this way, dynamic ET operation was emulated to characterize the transistor and optimize it with a systematic perspective.

Then ET was considered on this driver device and characterized by the above RF pulse sweep test to study its potential for ET application as shown in Fig.15 and Fig.16.

Fig.15 shows the measured efficiency of the GaN HEMT transistor at different supply biases as a function of CW output power. On each colour curve, a constant bias was employed, the efficiency decreased dramatically as the output power was backing off. However, ET operation will keep the transistor working on a dynamic envelope tracking drain efficiency trajectory, resulting in high efficiency over wide range of power levels. The maximum drain efficiency trajectory shape was dropping to some extent which might influence the ET overall efficiency. The highest drain efficiency point of trajectory happened on fixed supply 29V at 39.73dBm output, with peak efficiency 76.64%. Therefore,the more clipping to move signal PDF toward right would be needed for high overall efficiency for this part.

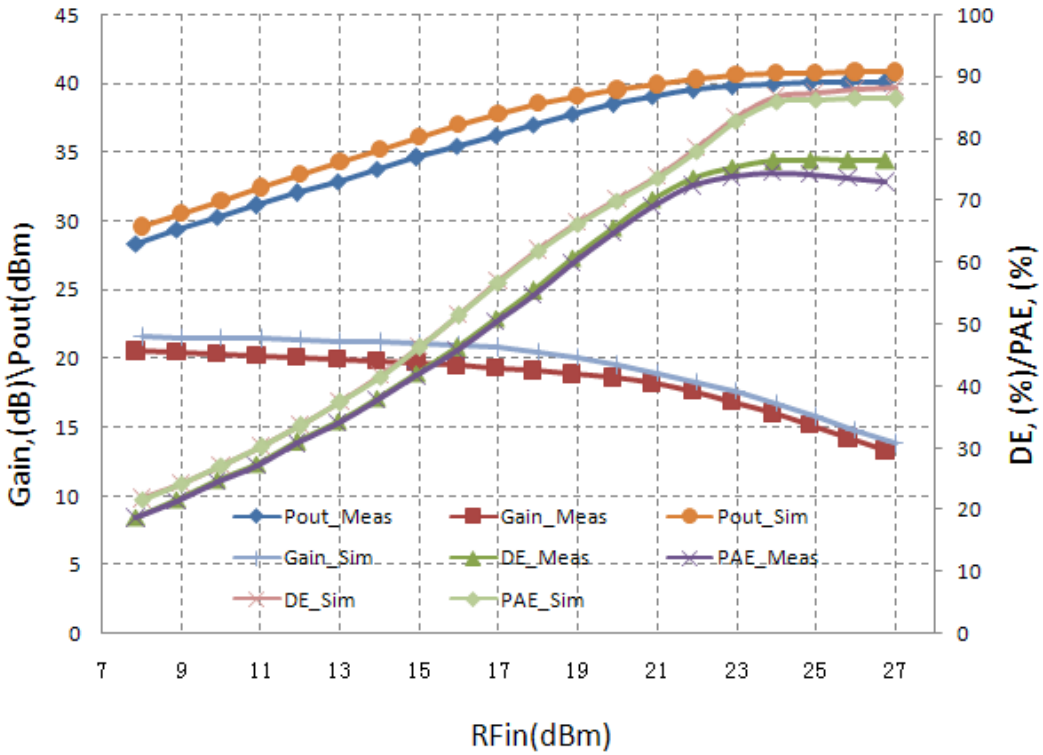

Figure 13. Measured power sweep test results compared to simulation data of the inverse class-F design at 2.14GHz

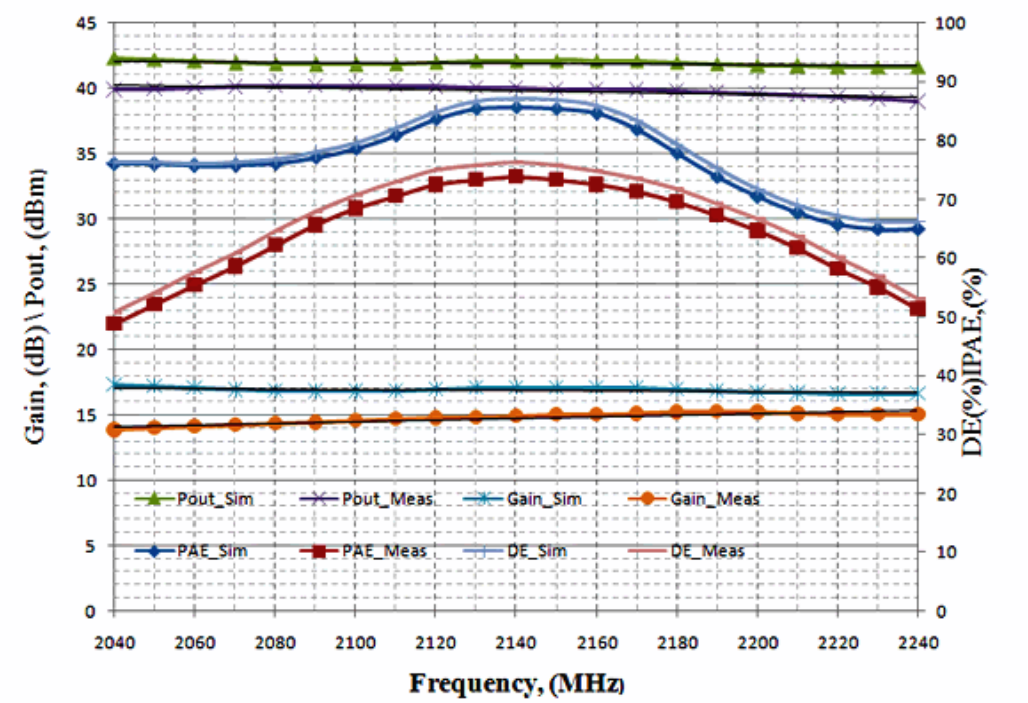

Figure 14. Measured frequency sweep test with 25dBm input level results compared to simulation data of the inverse class-F design at 2.14GHz

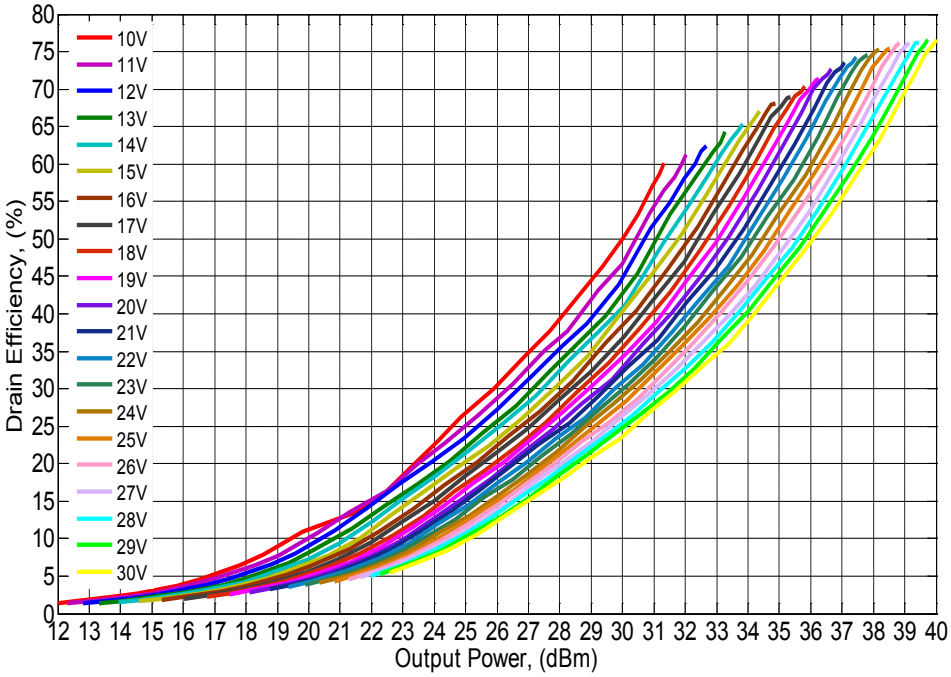

Figure 15. Measured inverse class-F driver ET drain efficiency trajectory with RF CW pulse amplitude sweep

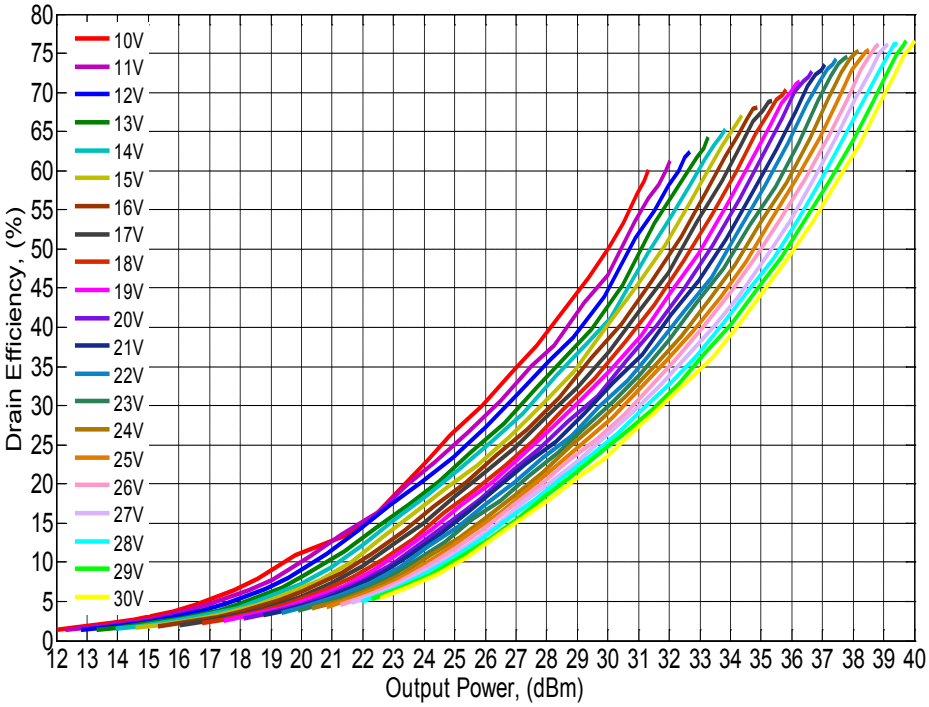

Figure 16. Measured inverse class-F driver ET gain efficiency trajectory with RF CW pulse amplitude sweep

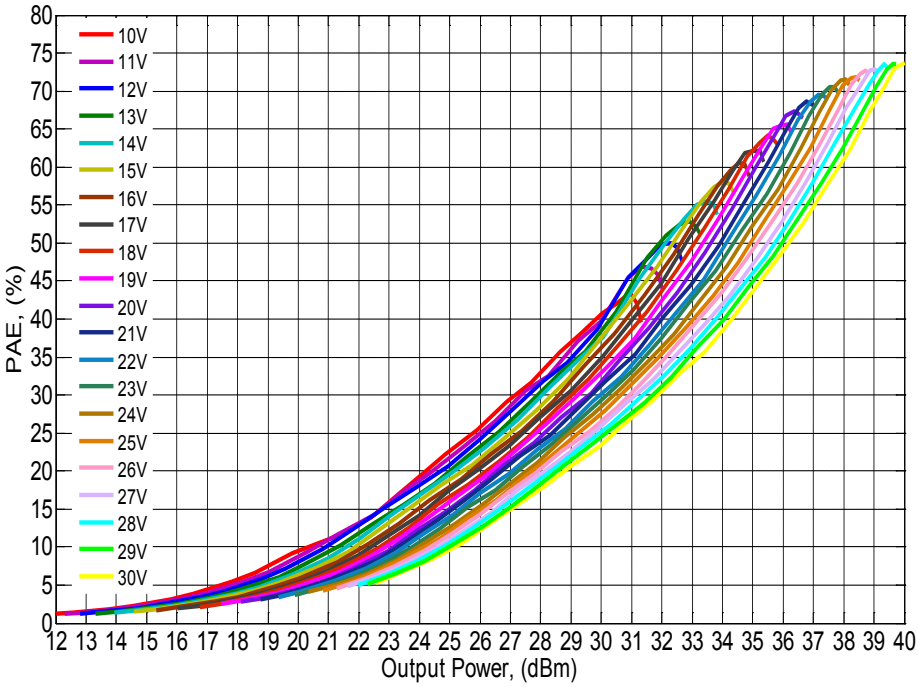

Figure 17. Measured inverse class-F driver ET PAE efficiency trajectory with RF CW pulse amplitude sweep

In the gain trajectory shown in Fig.16, the part had more drooping of gain, which was more obvious at high voltage range. From this point of view, the design would be possible to suffer a little bit more compression for high voltages.

However, the gain variations over drain biases were not neglect able, which indicated that it was possible to be less "linearizable" from pre-distortion capability perspective, especially for lower voltages during ET.

All above analysis and predictions were based on CW RF pulse sweep test, which were not the actual ET scenarios.

The serious gain variations ranging from high voltageand low voltage biases are not benefit for dynamic linearization during ET scenarios and may cause some PAE loss due to the gain drop at low voltages. By virtue of this worry, an PAE trajectory was implemented also to investigate the situations of PAE drooping in trajectory, especially at low voltage drain biases. The results were shown in Fig.17.

From Fig.17, compared to Fig.15, the PAE trajectory was indeed drooped to some extent than drain efficiency trajectory. Therefore, when apply ET, the lowest drain bias

should be controlled which must be higher than traditional values, which only consider higher than knee voltage to shutting down the transistor. ET operation on high voltage would benefit both overage line-up efficiency and linearization capability of the DPD engine. With this kind of driver amplifier applied, the adaptability of final stage should be carefully studied to make the optimized line-up operation.

Finally, to study the linearization capability of the inverse class-F driver, TI GC5325 DPD set was employed to performance the experiments with LTE 64QAM 20MHz signal, with the above proposed E-CFR clipped into 6.6dB PAPR, on 30V fixed drain voltage and 145mA quiescentcurrent bias. The results were shown in Fig. 18 as below.

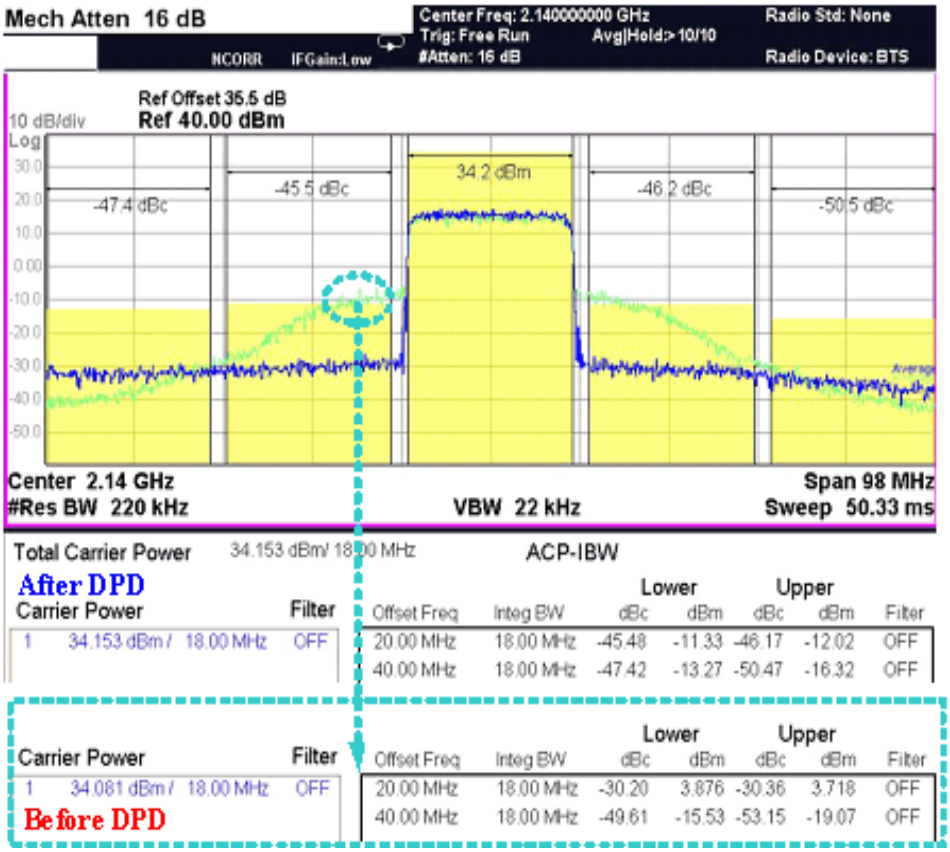

Figure 18. Measured PA output spectrum before and after DPD with 20MHz LTE signal, on 30V fixed supply

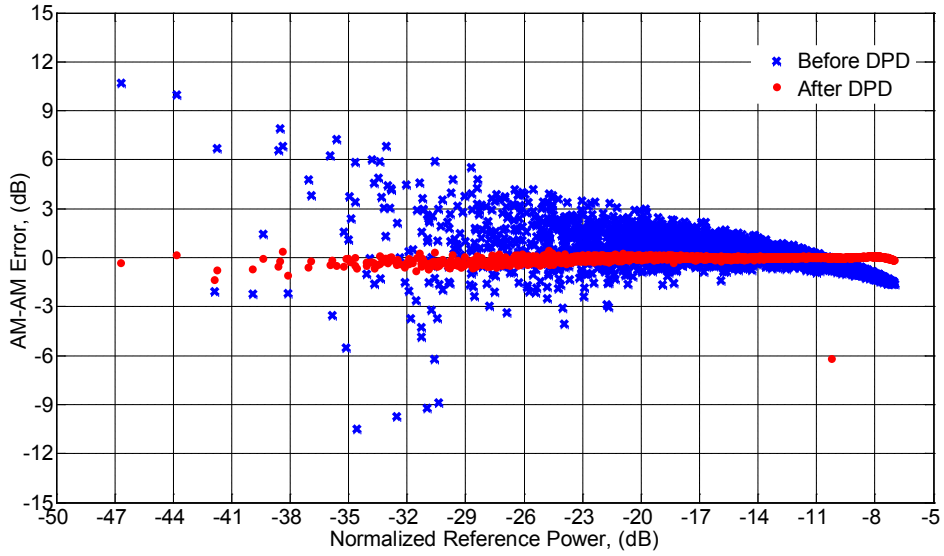

Figure 19. Measured AM-AM response before and after DPD with 20MHz LTE signal

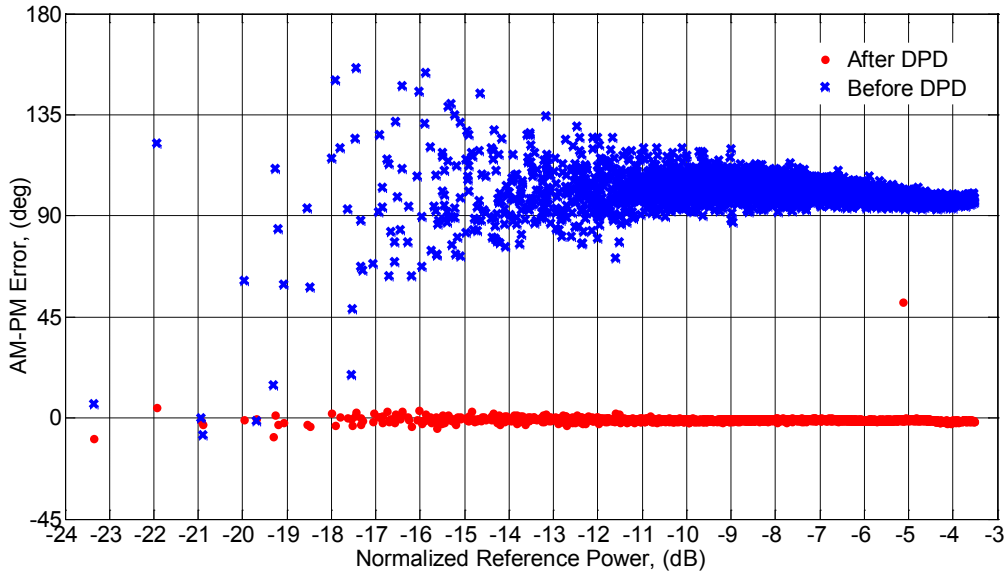

Figure 20. Measured AM-PM response before and after DPD with 20MHz LTE signal

Fig.18 showed the inverse class-F PA linearity, before and after DPD, in terms of the adjacent channel leakage ratio (ACLR) measured according to 3GPP LTE standard specifications. Before DPD, ACLR of -30.2dBc, whilst operating at 34.2dBm output power. When DPD was implemented and became stable, while kept the output power level the same, ACLR was -45.5dBc, kept approaching the threshold of 3GPP requirement of -45dBc, the efficiency was 44.8% with a power gain of 17.9dB, which was approximately 2dB compression.

While to run the design as driver to keep more linearity margin as possible, to keep ACLR below -50dBc, only 1.3dB back-off was needed to implement kept average output power as 32.9dBm, linearized ACLR being -50.1dBc, with efficiency as 39.9% with power gain 18.6dB.

Therefore, good linearization capability for DPD was observed from the experimental results. For more details of the memory effect, in terms of AM-AM and AM-PM characters of the inverse class-F, experiments were implemented with the same modulated LTE 20MHz signal. The results were shown in Fig. 19 and Fig. 20 with red dot to stand for results after DPD and blue cross 'X' to stand for the results before DPD.

From above results, both amplitude and phase error could be compensate well with DPD of the inverse class-F design, which clearly showed that the design was quite linearizable with fixed 30V drain supply. For ET operation, the supply modulator discussed in section III was utilized to supply power. Both wide band voltage and current probes are used also to monitor the drain voltage and current to observe the efficiency boosting due to drain modulation supply.

With average output power 33dBm, power gain dropped into approximately 14.8dB due to ET, ACLR1 was -41.6dBc and ACLR2 was 43.2dBc, drain efficiency was boosted up to 72.5% from 39.9% at fixed 30V supply, excluding efficiency of ET modulator.

To make compliance to 3GPP requirement, keeping ACRL1 as -46dBc and ACLR2 was -50.5dBc, the output power was dropped into 32.3dBm, while drain efficiency was 64%, excluding efficiency of ET modulator.

6. Conclusions

In this paper, comprehensive design considerations for multi-stage envelope tracking power amplifier line-up was analysed and concluded. The benefit of lining up ET amplifiers over other topologies are obvious and it could make more profit in a radio system by cutting overall costs due to higher efficiency with higher PAE. The line-up PAE character was analysed that it produced a constant PAE response varied with driver amplifier collector or drain efficiency, superior to single final stage solution. In section III, the wideband ET modulator with nested structure was introduced to further boost modulator efficiency. E-CFR was proposed to reduce both the peak and composite EVM of LTE signal during clipping, which could make the PDF more fit for the ET efficiency trajectory. Also, a 10W inverse class-F driver amplifier based on GaN HEMT was implemented with good linearization capability. With 30V fixed supply, when DPD was implemented and became stable, while kept the output power level the same, ACLR was -45.5dBc, kept approaching the threshold of 3GPP requirement of -45dBc, the efficiency was 44.8% with a power gain of 17.9dB. When the amplifier was implemented with ET, kept the linearity specifications, drain efficiency was boosted from 39.9% to 64%, excluding efficiency of ET modulator.

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