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Novel Digital Pileup Inspection Circuit for a Gamma Ray Spectroscopy System

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Abstract Apart from the noise associated with an incident radiation pulse, other sources of error in nuclear radiation measurements are from the dead time required for the processing of the pulse and the pile up of pulses. The schemes employed in analogue processing still result in appreciable errors in the observed results while digital schemes are complex and expensive for most laboratories especially in developing countries. We have designed and implemented a cheaper digital nuclear radiation processing system that will significantly reduce these problems of errors in nuclear spectroscopy. The processing scheme is based on digital pulse processing in both slow (energy) and fast (inspection) channels. The output of the fast channel is used for pileup inspection and slow channel peak capture while the slow channel itself provides for the accurate pulse peak determination required for good energy resolution. The dead time effect is only restricted to the slow channel processing time which is the same as the pileup inspection time. The system functions in a non paralysable dead time effect manner with an appropriately derived dead time and pileup error correction function.

Keywords Dead Time, Digital Processing, Error Correction, Peak Detection, Pileup Inspection

1. Introduction

In any nuclear radiation processing system where noise is present and is capable of triggering the detection electronics or algorithm, it is not sufficient to simply count the triggering events and use assumptions about the distribution of arrival times to make pileup loss corrections in order to determine the incident rate of x or gamma rays on the detector. It is necessary to understand the nature of the rejected events and their distribution [1]. The time interval which is required to process one pulse or event is called the dead time, implying that the system is dead to process another pulses or events during this time interval. It is assumed that each pulse occurring event is followed by a fixed dead time interval t. Thus, an important source of error comes from this finite time required by the counting electronics to detect and process radiation pulses. Dead time losses may be compensated very well by the pulse-height analyzer, but pileup losses may not be [2]. The dead time is really due to the resolving time associated with the detector itself, its amplifier and the time required to convert the pulse to a digital form used for spectroscopy. During this dead time, the system cannot respond to other photons that hit the detector and these events will not be counted and thus are lost [3]. Depending on the behavior of a system, two kinds of dead-time can be distinguished: extended (or paralysable) and non-extended (or non-paralysable) dead time. In the case of an extended dead time, an event occurring during the time t belonging to a previous pulse, although it will be lost, still starts a new dead-time period. That is, it extends the dead time. In the case of a non-extended dead time, an event occurring during the dead time interval is lost and does not start a new dead period [4]. Pileup loss arises due to the fact that two radiation pulses may arrive close to themselves in time with the result that their values overlap and are summed up such that the new summed value does not represent any of the two pulses. This constitutes serious distortions to the accuracy of measured pulse values.

Many laboratories still use gamma ray spectroscopy systems still employ analogue schemes to implement the processing of radiation pulses while digital schemes are used to interface the analogue processor to the computer. The effects of dead time and pileup errors are often down-played in these systems, leading to serious errors in the observed results. An alternative is the use of digital processing systems but the popularly available ones employ complex mathematical schemes such as adaptive trapezoidal/ triangular filtering, symmetric or asymmetric cusp-like weighting and others. Such schemes require complex data operations such as digital multiplications, exponentiations, look-up tables for weighting functions, data set buffering for both time variant processing and inter-process synchronization in addition to complex dead time and

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pile-up error correction functions [5,6,7]. These are expensive to implement in terms of the processing times and costs of the required electronic components. In order to reduce these losses without compromising on the efficiency of the spectrometry, we have designed a relatively cheap, simple and much more accurate computer controlled gamma ray spectroscopy system for laboratory uses especially in developing countries. We have also derived an appropriate simple correction algorithm for the determination of accurate radiation counts [8].

2. Description of the Digital Measurement System

Figure 1 shows the block diagram of the digital nuclear radiation measurement system incorporating the implemented pileup inspection circuit. The circuit blocks in the dashed box 1 constitute the main processing system which includes the filter, peak detection and pile-up inspection (FPPI) circuits such as in the progenitor of more complex and expensive commercial products [6,7]. It is noted that the digital filters and their associated noise threshold circuits may become necessary for further noise reduction especially at high count rates. However, at low count rates, they may be omitted from the system if the input to the digital processing system is obtained from an already processed pulse such as from a detector-preamplifier unit or an analogue pulse shaping amplifier.

The Analogue Signal Conditioner (ASC) is contained in the dashed box 2 and includes the input amplifier stage and the Analogue-to-Digital Converter (ADC). It shapes and converts the incoming radiation pulses to appropriate digital forms for further digital processing. Included in the ASC also are the clock and counter section that provide the necessary timing clock pulses for the various circuits. The ASC also includes the analogue pulse generator (APG) which provides a slow pulse (STP) of width equal to the pulse width of the input radiation pulse and a very short time pulse (FTP) needed for the inspection of pile-up of pulses. The computer interface circuit (CIC) interfaces the main processing section to the computer. The operations of the ASC, CIC and the FPPI are controlled by the computer through appropriate interface software.

The function of the pileup inspector is to ensure that the slow channel pulse outputs are sampled only when the captured peak values result from a good pulse event. A good pulse event is one which results from a pulse that is separated from both its predecessor and successor by a time interval that is at least greater than the slow channel's peaking time or pulse width. That is, a good pulse must be free of both leading edge and trailing edge pileups [9]. Pileup inspection is implemented in such a manner that considers the only three possible conditions that could lead to pile-up situation.

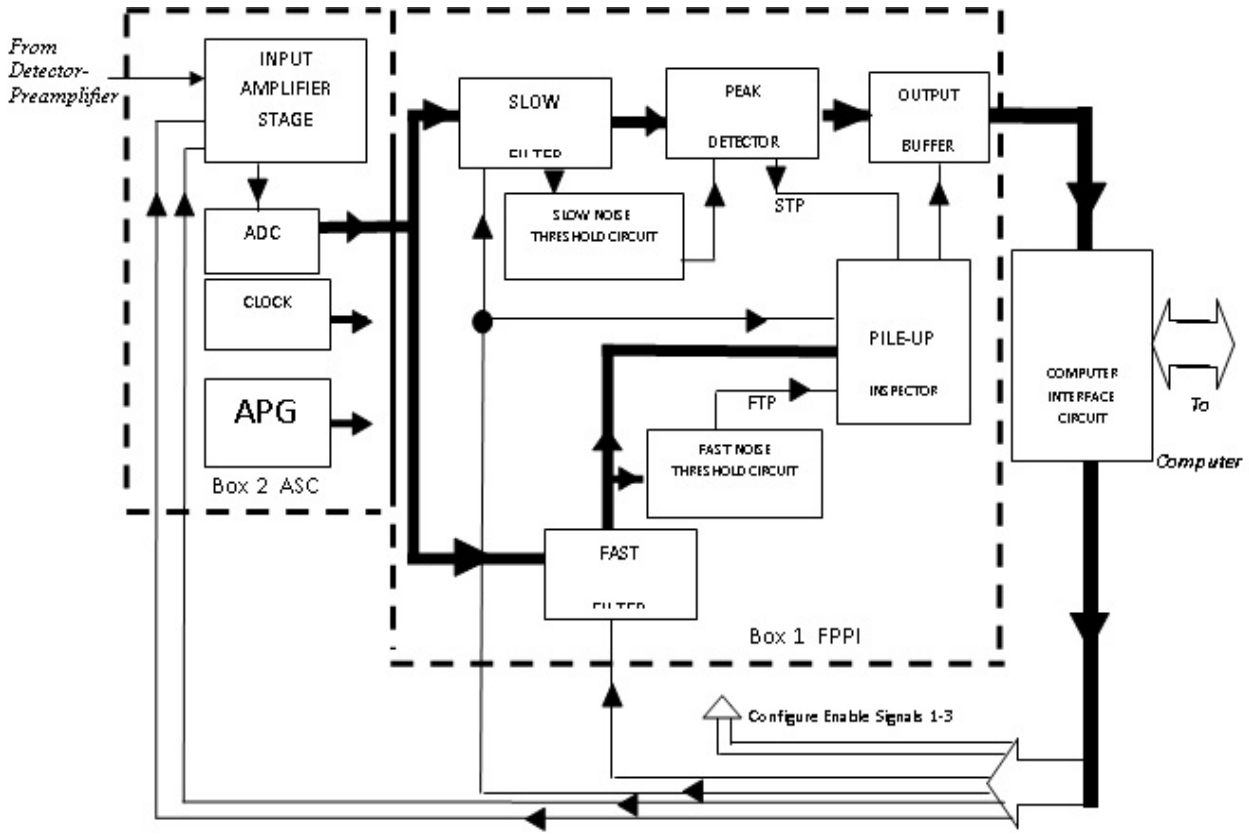

Figure 1. Diagram of the measurement system with the component blocks

In the absence of the digital filters and their associated noise threshold circuits, ie, at low count rates and when the input to the system is taken from a detector-preamplifier unit or an analogue pulse shaping amplifier, the FPPI operates slightly different from when digital filters are used. Firstly, the ADC output is sent only to the slow channel. Secondly, the input to the fast channel is the fast pulse from the APG while the slow channel's pulse width could serve as the pile-up inspection time. Finally, when digital filters are used, the adjustable digital parameter loaded into the FPPI is the digital filters' peaking time values while for the detector-preamplifier or analogue pulse shaping amplifier, the loaded parameter is the pulse width.

3. Pileup Inspection

Figure 2 shows a schematic diagram of a simple and efficient digital pileup inspection circuit which functions in a non-paralysable dead time manner. This approach both simplifies its operation and its count rate correction techniques using the non-paralysable dead time function. Here, the slow channel and fast channel pulse shapers are used to achieve an efficient pileup inspection scheme. As will be obvious from the discussions on its functioning and the considerations of the only three possible conditions, there are no separate slow and fast pileup situations.

On one hand, when a detected radiation event occurs, the fast channel filter output will be applied to the input of the fast noise threshold circuit (FTC) as shown in the block diagram of Figure 2, causing an output pulse FTP with a pulse width equal to the time that the magnitude of the fast filter signal exceeds the FTC noise threshold. The slow channel noise threshold pulse STP derived from the peak detector circuit is used to trigger the loadable down counter DC to count down to zero from the loaded value of the pileup inspection time PIT which is chosen to be equal to the peaking time of the slow channel filter.

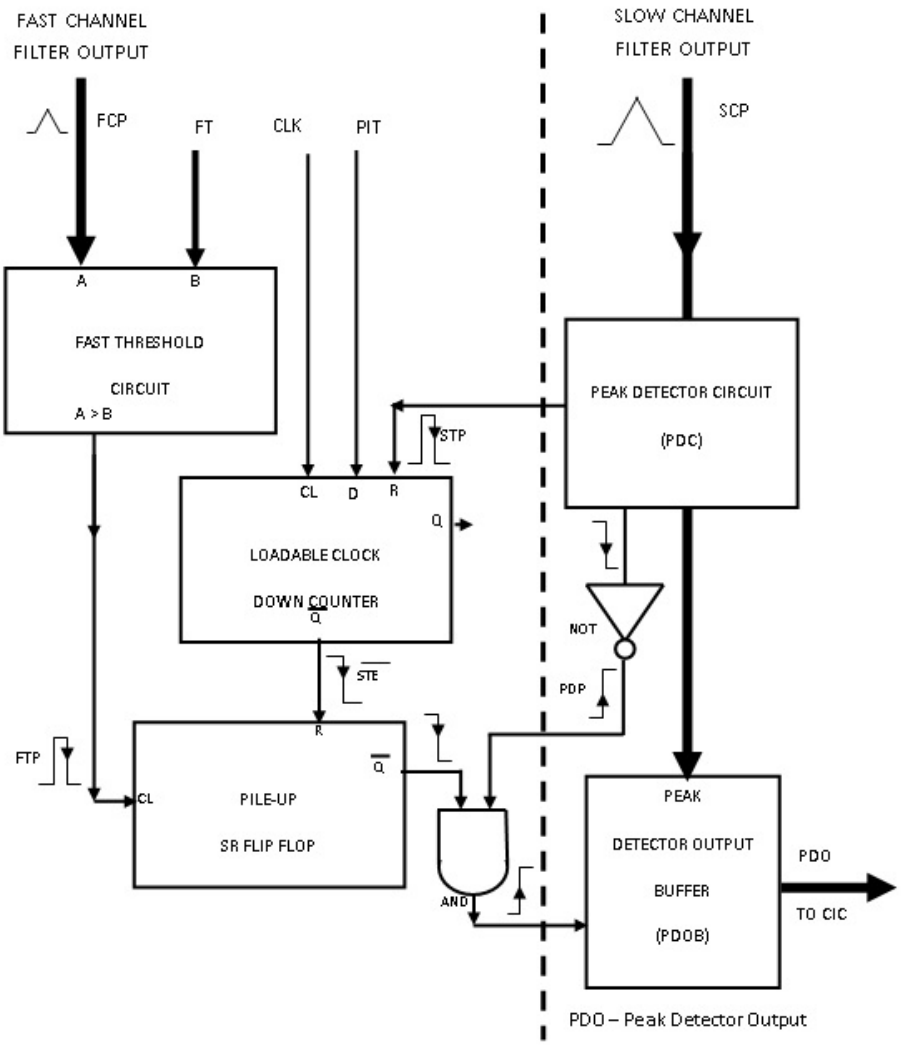

Figure 2. Block diagram of peak pileup inspector

On another hand, when a detector-preamplifier or an analogue shaping amplifier is used, then the ASC amplifier output will be applied to the input of the APG causing an output pulse FTP with a pulse width equal to the time that the magnitude of the ASC amplifier output signal exceeds the APG noise threshold. The slow channel pulse STP derived from the same APG circuit is used to initiate the capture of the peak value of an incident radiation pulse. It can also be used to reset the pileup flip-flop FF. In this mode and as long as it is present indicating the presence of a pulse being processed, any other pulse arriving within the duration of its presence will cause the output of the flip-flop FF to go LOW, thereby disallowing the recording of any peak value. The triggering of the loadable down-counter DC to count down to zero from the loaded value of the pileup inspection time PIT, is achieved through the triggering interface of Figure 3.

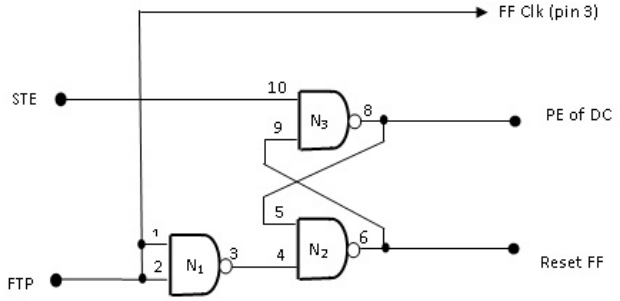

Figure 3. Triggering interface circuit

The fast threshold pulse FTP produced in the APG is used to clock the pileup flip-flop FF. It is also inverted in N1 of the triggering interface. As soon as the output of N1 goes LOW, the output of N2 goes HIGH. Since the output of N2 is connected to one input of N3 and the other input of N3 is usually HIGH until counted down to zero, the output of N3 will go LOW. Even after the output of N1 goes HIGH, N2 output remains HIGH until the loadable down counter has counted down to zero. Immediately, STE signal goes LOW thereby outputting a positive going reset pulse at N3 output to reload the PIT value in the DC. The alternate output of N2 can be used to reset the pile-up flip flop FF.

Normally the loadable down counter DC (Figure 2) holds the pileup flip-flop FF in reset condition so that its output applies a high input to AND gate. When the loadable down counter DC starts counting down, the reset voltage is removed from flip-flop FF. If there is another fast threshold pulse FTP during the DC down counting, the leading edge of that fast threshold pulse can clock the flip-flop, causing the output to go LOW. When there is no other fast threshold pulse FTP and DC is counting down, the output of the AND gate is used to enable the peak detector output buffer PDOB as soon as the peak detect pulse (PDP) is present, thus transferring the captured peak value of the slow channel to the computer interface circuit (CIC) for further processing.

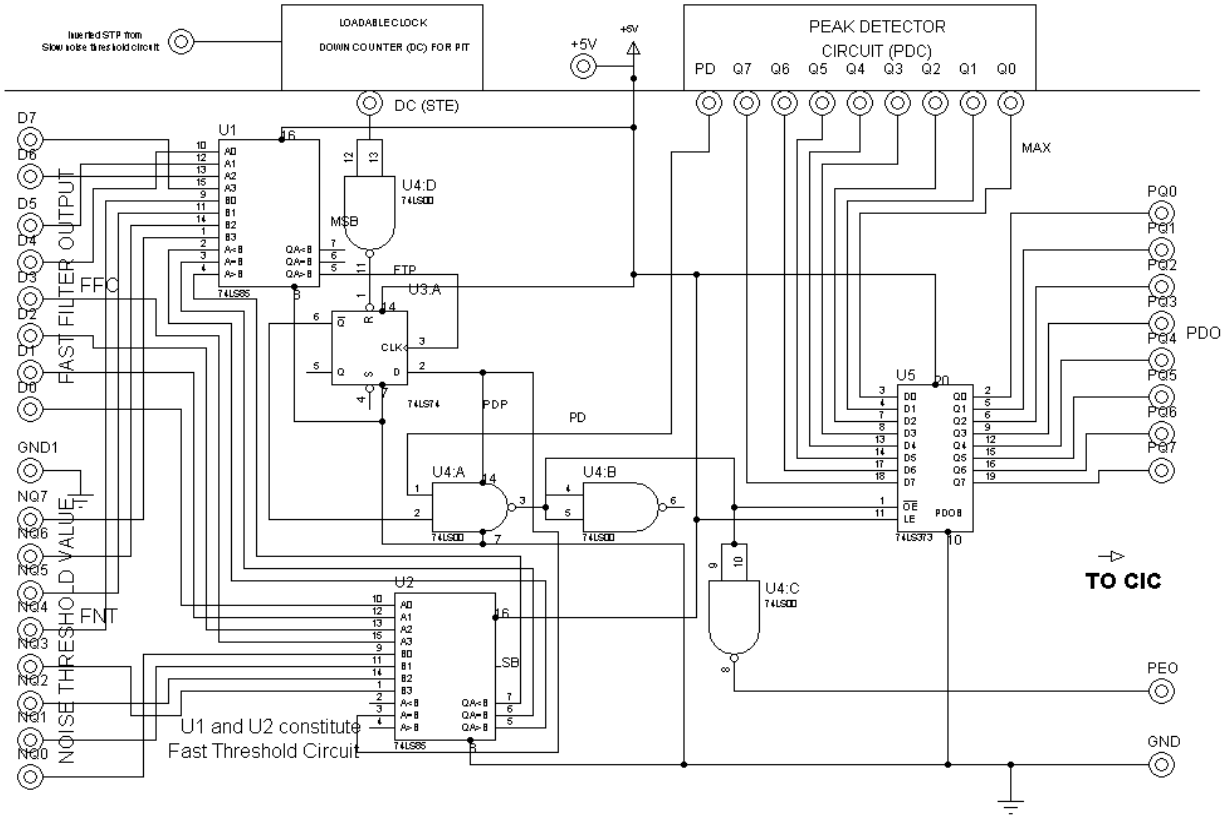

Figure 4. Peak pileup inspector

The implemented pileup inspection circuit is shown in Figure 4. When a detected radiation event occurs, the analogue pulse generator (APG) of the ASC produces an output pulse FTP with a pulse width of about 4 μS. The inverted form of the slow channel noise threshold pulse STP derived from the APG circuit is used to trigger the pileup inspection time (PIT) loadable down counter DC to count down to zero from the loaded value of the PIT. The PIT is chosen to be equal to the peaking time of the slow channel filter or equal to the pulse width of an input pulse.

Normally the PIT loadable down counter DC holds the pileup flip-flop U3A in reset condition through STE so that its output applies a high input to NAND gate U4A. When the PIT loadable down counter DC starts counting down, the reset voltage STE is removed from the flip-flop U3A. If there is another fast threshold pulse FTP during the PIT DC down counting, the leading edge of that fast threshold pulse will clock the flip-flop U3A, causing the output to go LOW. This also causes the output of NAND gate U4A to go HIGH, thus preventing the peak detector output from reaching the output of the peak detector output buffer (PDOB) U5 irrespective of whether the peak detect signal is HIGH or LOW.

When there is no other fast threshold pulse FTP and PIT DC is still counting down, as the output of the pileup flip flop U3A is still HIGH, as soon as the peak detect pulse (PD) goes HIGH, the output of the NAND gate U4A goes LOW and is then used to enable the PDOB which now allows the peak detector output to reach the output of PDOB, ie PDO. From here, PDO is sent to the computer interface circuit (CIC) for further processing. Eventually, the PIT DC will count down to zero and hold the pile-up flip-flop U3A reset pin HIGH until another detected radiation event takes place.

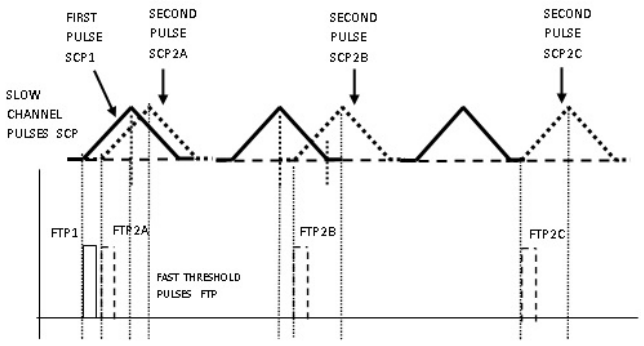

Figure 5. Pileup test conditions

The pileup inspector considers possible arrival times of pulses and hence, inhibits interfering output pulse peaks while allowing non-interfering pulse peaks to pass through. Figure 5 illustrates how the pileup inspector will inhibit interfering output pulse peaks (pileup condition) while allowing non-interfering pulse peaks to pass through. The sketch shows the occurrence of an initial slow channel pulse SCP1 and a second slow channel pulse SCP2 occurring at three different times after the initial slow channel pulse. Due to symmetrical nature of the triangular shaped pulse, only three conditions for pileup can be distinguished and the circuit tests for these conditions.

a. Test condition 1 considers a situation where the start of the second slow channel's pulse SCP2 occurs during the rise time of the first pulse SCP1 and the peak of the second pulse occurs during the fall time of the first pulse. It is clear that the peak amplitudes of both the first and second pulses SCP1 and SCP2 are each affected by the other pulse. Hence, both pulse peaks are rejected to prevent pulse interferences. In this condition, the fast channel pulse FCP corresponding to the first slow channel pulse will cause the fast threshold circuit FTC to generate pulse FTP1 to enable PIT DC. The down counting of PIT DC removes the reset voltage from pileup flip-flop U3A. With the next detected event occurring during the rise of the first slow channel pulse SCP1 (half of PIT), a second fast channel pulse will be generated and a second fast threshold circuit pulse FTP2A will be produced. Since this second fast threshold circuit pulse FTP2A occurs during the down counting of PIT DC, the front edge of the second fast threshold circuit pulse FTP2A will clock the flip-flop U3A, causing it to output a LOW signal to NAND gate U4A. This LOW state will be maintained until flip-flop U3A is again reset. With time and as the peak detector output signal peaks at about half of PIT, and with the pileup flip-flop U3A holding one input of NAND gate U4A LOW, the peak detector pulse PD has no effect in enabling the peak detector output buffer PDOB. If no further detected signal occurs, the PIT DC will count down to zero and hence, reset the pileup flip-flop U3A, which then holds one input of NAND gate U4A HIGH again.

b. Test condition 2 considers that the second slow channel pulse SCP2B starts after the peak of the first pulse SCP1 and peaks after the first pulse ends. In this case, none of the two pulses interferes with the peak of the other pulse and output signals corresponding to both peaks are produced. Consequently, the pileup flip-flop U3A will hold NAND gate U4A input HIGH so that the peak detector pulse PD occurring at about half of PIT, will through the NAND gate U4A, enable the PDOB output to be sent to the CIC. The second fast threshold pulse FTP2B will occur after the PIT DC has counted down to zero, which in turn will cause a reset voltage to be applied to flip-flop U3A. With flip-flop U3A now held in reset condition, it cannot be clocked by the second fast threshold circuit pulse FTP2B.

c. Test condition 3 considers the situation where the second slow channel pulse SCP2C does not begin until after the first slow channel pulse ends. Since neither pulse affects the peak of the other, separate output pulses are allowed through. Thus, since the second fast threshold circuit pulse FTP2C does not occur until after the first pulse of the down counting of PIT DC, the pileup inspector circuit operates as in the case of test condition 2.

4. Performance Analysis of the Circuit

The designed digital pileup inspection circuit is required to minimize the effect of pileup of pulses and dead time in the measurement of nuclear radiation. This effect is drastically reduced through the technique of eliminating all other pulse processing timings and delays except that for processing a pulse which is the same as checking for pileup of pulses. This technique and the elimination of piled up pulses are achieved with the combined operation of the digital difference-type peak detector (DTP) [10] and the pulse pileup inspector (PPI) circuits. The errors due to the dead time and pileup of pulses can be compensated through an error correction function that has been developed for this non-paralysable dual-channel digital nuclear radiation pulse processing system [8].

Figure 6. Interconnections of the circuit boards

The interconnections of the various circuit blocks allow for in-circuit testing as shown in Figure 6. To analyse the designed digital circuit, it is required that the output of the analogue signal conditioner (ASC) should be typical nuclear radiation detector-preamplifier and shaping amplifier's pulse shapes and values. Hence, for the popular gamma ray spectroscopy system, the input to the ASC should be the output of the ORTEC 276 scintillator-detector with preamplifier base or ORTEC 575A pulse shaping amplifier. The output of the ORTEC 276 preamplifier base is a pulse of time constant of 50 μS while the output of the ORTEC 575A pulse shaping amplifier is a triangular-like shaped signal [11,12]. Since in-circuit testing cannot be carried out with the actual radiation source and associated preamplifier/pulse shaping amplifier, testing was done with simulated outputs of both the preamplifier and pulse shaping amplifier using the circuit of Figure 7. For the preamplifier pulse output, the input to the circuit is a rectangular waveform while for the output of the pulse shaping amplifier, the input is a sinusoidal waveform. The amplitude of the input waveforms may vary from 0.1 V to 10 Vp-p while its frequency can range from below 1Hz to over 50 KHz.

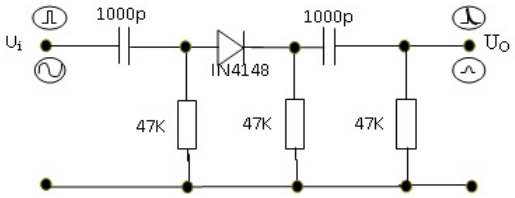

Figure 7. Simulated Output Shapes of Preamplifier/Pulse Shaping Amplifier for Testing the ASC and Digital Triangular Filters

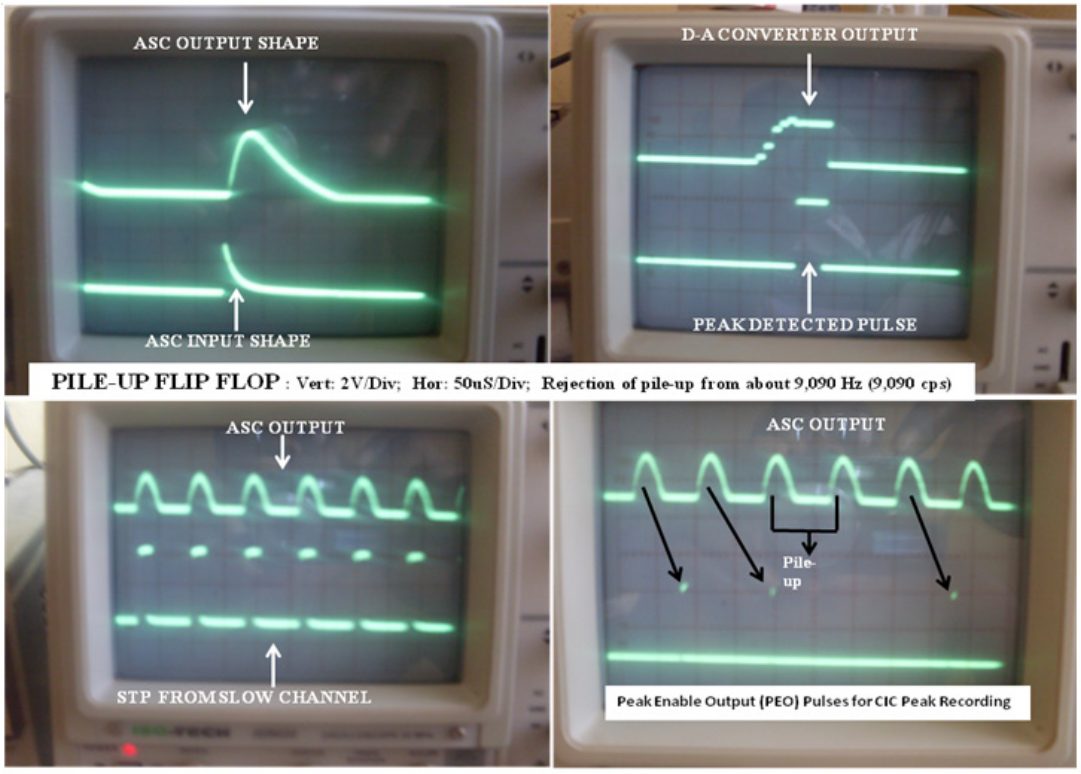

Figure 8. ASC, Peak Detector and Pileup Waveforms

The peak detector waveform in response to an analogue signal input is shown not on the same scale, in Figure 8. An important waveform from the DTP is the Peak Detect (PD) pulse which signifies the presence of a pulse peak value at the digital outputs of the DTP. A typical example of such digital peak value is shown as the local D-A converter output. For the analysis of the PPI, the pulse amplitude of Figure 7 is about 4 V with a time constant τ =RC of 47 μS. The corresponding analogue amplifier output varies from a value of 2.8 V at below 1 Hz to about 0.4 V at over 10 KHz. The PPI waveforms in relation to the analogue amplifier output are also shown in Figure 8. The fast threshold pulse (FTP) has a width of less than 4 μS. This width ensures that the pileup inspector circuit functions up to a maximum slow threshold pulse (STP) width of about 4 μS, an equivalent count rate of 250,000 cps. A typical pileup situation occurs as shown in Figure 8. This is shown by the waveform at Pin 6 of the pileup flip flop FF. Without pileup, Pin 6 of the FF will be at high voltage level, enabling the pulse enable output signal PEO to reach the computer interface circuit (CIC). As soon as pileup is present, the Pin 6 voltage goes low, disabling the PEO signal from reaching the CIC. The application of dead time and pileup correction would further compensate for the dead time and pileup effects, which is not obtainable with most popular analogue systems.

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