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Effective Elimination of Analog Impairments Error in Parallel Interleaving Sigma Delta A/D Converters

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Abstract The oversampling sigma delta modulators which produce one bit samples of input signals can be used to create AD converters, which can produce either multi bit samples of high resolution but with low sampling frequency, or low resolution samples with high sampling frequency. One of the methods of overcoming this limitation is based on using several converters operating in parallel in a time interleaving manner. This way the resolution of the converter digital output can be significantly increased i.e. the quantising error value reduced. However the analog impairments of parallel converters cause modulation of the output samples which can significantly deteriorate the resultant converter properties. Somehow in many papers describing various structures of Σ-Δ AD converters analysis is limited to the frequency domain, ignoring the fact that Σ-Δ modulators are in fact synchronous voltage to frequency converters. This paper demonstrates how, recognizing the time domain properties of Σ-Δ modulators, the problem of analog impairments of converters can be overcome resulting in a better design of high resolution Σ-Δ AD converters.

Keywords Parallel sigma delta converters, Resolution, Sampling, Interleaving techniques

1. Introduction

The sigma-delta (Σ-Δ) AD converters are nowadays the most popular choice employed in digital audio systems and in high-resolution precision industrial measurement. In the digital audio systems the flat distribution of quantising error, achieved by using sigma delta modulators of higher order, is relevant as it eliminates the idle tones which appear in the audio outputs. Therefore, taking into consideration the distribution of quantising errors, the majority of existing papers presents analysis of various Σ-Δ AD converters in frequency domain ignores the time domain properties of Σ-Δ modulators.

However in the industrial digital system only the magnitude of quantising error is important, and taking this into consideration the Σ-Δ modulators can be viewed [1] as a synchronous voltage-to-frequency converter followed by a counter. If the number of "1"s in the output data stream is counted over a sufficient number of clock pulses, the counter output will represent the digital value of the input.

Remembering this, the relevant improvement of properties of the parallel structure Σ-Δ AD converters can be achieved, what is presented in this paper.

Generally the main advantage of Σ-Δ AD converters is that the digital output of them can be of very high, theoretically unlimited, resolution. However to obtain high resolution of the output digital words the counting time requires many clock pulses which results in a low sampling rate. Using a single Σ-Δ converter, of any order, it is not possible to have both high resolution and high sampling rate.

The idea was then conceived to provide additional samples in between high resolution samples by using additional Σ-Δ converters working in parallel.

Many concepts of parallel Σ-Δ converters have been described in the literature [2], [3], [4], [5]. The majority of these basically rely more or less on the concept of interleaving ADCs described in [8].

A block diagram showing the basic idea of such a parallel converter is shown in Fig. 1.

An analog input signal V_{IN} is sampled simultaneously by a number N of ADCs. ADC_1 will sample V_{IN} first, starting at (t_0) and begin converting it into an n-bit digital representation, m clock pulses later and before the conversion of ADC_1 ends, ADC_2 will start sampling the input at (t_0 + T), where T=mτ and τ is the clock pulse duration, and begin converting it again into an n-bit digital representation. Then, another T seconds later, ADC_3 will sample V_{IN} at (t_0 + 2T) and so on. Before ADC_N has finished sampling it started at (t_0+NT), ADC_1 at [t_0+(N+1)T] immediately restarts sampling and the whole cycle of sampling is repeated.

As the n-bit outputs of the ADCs become sequentially available, the digital n-bit samples sequentially appear at the converter output D_{OUT}.

If the fixed conversion time of each individual ADC is

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denoted by M, then if only one ADC operates in the system the sampling rate equals 1/M. When N interleaved ADCs operate in the described above manner, the effective sampling rate is N times higher i.e. N/M.

This powerful technique makes possible a significant increase in the sampling rate of the Σ-Δ AD converter whilst keeping high converter resolution. However the interleaving technique is not free of practical challenges, as described in [8].

The analog impairments in the numerous channels of ADCs cause modulation of the output samples, leaving "interleaving spurs", which are equivalent to the presence of additional components in the output signal spectrum. The spectral degradation of the output does not depend on the absolute value of the channels' impairments (amplifiers gain and offset), but on the relative mismatches/differences between them. The timing spurs, which might appear, when the consecutive channels sample a bit earlier or later than they should in the intended order, can be eliminated by using single clock to operate all of the converters, but there is no effective solution to eliminate problems caused by the analog impairments of the channels if more than one Σ-Δ modulator is used in parallel AD converter.

To illustrate how the analogue impairments of Σ-Δ AD converters cause modulation of the output train of samples Fig. 2 presents case of only two converters working in parallel.

Assuming that the input voltage is constant and the second converter, due to analogue impairments, produces samples of higher values, the resultant train of combined samples shows clearly magnitude modulation. Such a modulation of the output train of samples should not be present, as the input voltage is assumed to be constant.

Various techniques have been proposed to get rid of this problem i.e. to compensate or cancel residual spurs via randomization or other techniques, sometimes very complicated. In the following section a different and simple method is proposed as a solution to this problem.

The analogue impairments influence only the Σ-Δ modulators, which are the only analogue blocks of A/D converters. If each of the parallel converters have its own modulator than e.g. different voltage gain of its amplifiers, or the offset voltage, might cause different count of the output counters. If it possible to create a parallel Σ-Δ AD converter using only one common modulator to serve all of the parallel converters than the impairments effect would be eliminated, as the remaining parts of each of the converters are digital counters. Even if the amplifier of the single modulator is not perfect, the output samples of all counters will be of the same magnitude and the modulation shown in figure 2 will not be present.

Remembering that the Σ-Δ modulator can be viewed as a synchronous voltage-to-frequency converter, it seems that, such a solution can be implemented.

2. Theoretical Consideration

Let us consider the structure of a single channel of a typical Σ-Δ AD converter in the form shown in Fig.3 which is commonly used [9].

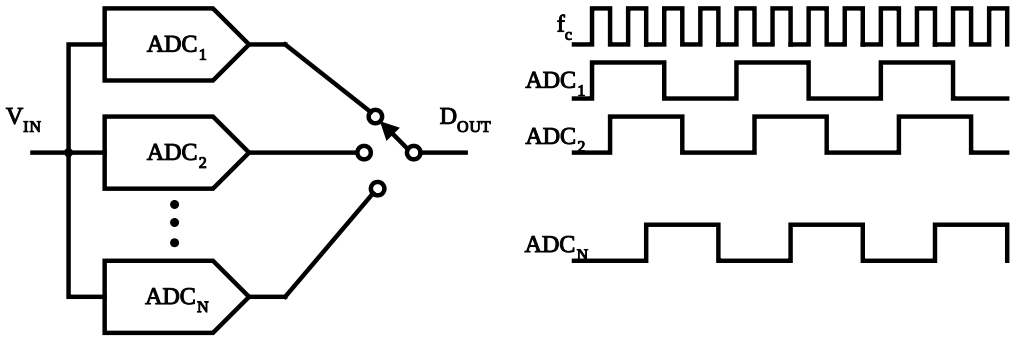

Figure 1. An array of N time interleaved n-bit ADCs [1]

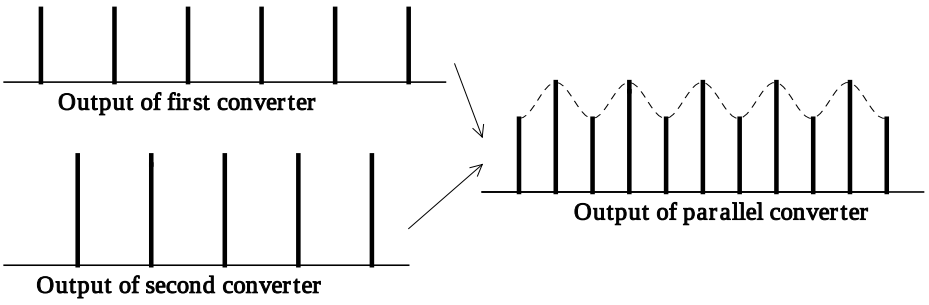

Figure 2. Analogue impairments (gain) of two Σ-Δ AD converters, working in parallel cause magnitude modulation of the output train of samples

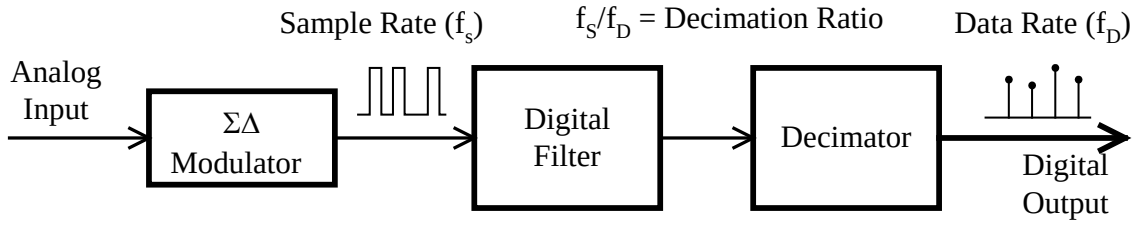

Figure 3. Block diagram of typical structure of a single channel of a Σ-Δ AD converter presented in literature [4, 5]

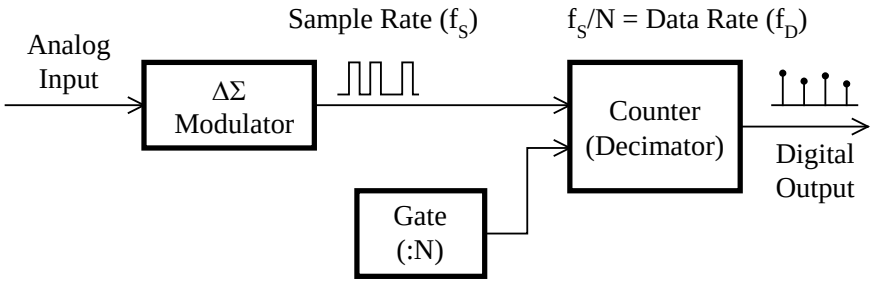

Figure 4. Simplified block diagram of a single channel of a Σ-Δ AD converter with digital filter and decimator replaced by series input parallel output counter

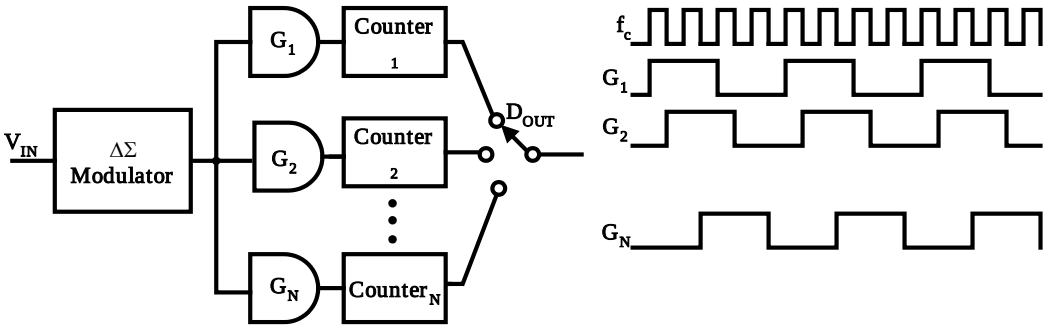

Figure 5. Modified structure of the array of N time interleaved n-bit ADCs

The output of Σ-Δ modulator is an irregular train of one-bit samples of the analogue input signal and the number of samples in a certain period of time represents the value of the input signal.

The digital filter, placed in the position shown in Fig.3, cannot perform any operation other than change the distribution of the output pulses of the modulator. The density of pulses must remain unchanged, as it contains information of the input signal magnitude. Therefore decimation must take place before any digital filtering is applied.

Decimation in this case should be understood as the simple counting of the number of pulses during a chosen time interval, which determines the decimation ratio and resolution of the output digital multi-bit samples of the input. The simple series-input, parallel-output counter should provide the required decimation, but it can be also treated as a low – pass digital filter of FIR type. The block diagram of the basic structure of a single channel of a Σ-Δ AD converter should then be simplified as shown in Fig. 4 in opposite to the structure presented in Fig. 3.

The Sigma Delta Modulator in Fig.4 can be of any order. It produces a stream of pulses applied to the counter through the timing device which determines the resolution of the output sample.

It can be easily proved that the counter itself, apart from being a decimator, acts as a digital filter of FIR type [10].

The output samples of such an Σ-Δ AD converter appear at the frequency $f_0 = f_s/N$ rate, where f_s is the frequency of modulator clock, and N is the number of f_s pulses gating the counter and fixing the resolution of output samples.

The sampling frequency f_0 can be increased by employing the concept of parallel connection of few single Σ-Δ AD converters, but instead of the complete converters with modulators it is sufficient to use only parallel counters, as shown in Fig. 5, gated in the same interleaving pattern as shown in Fig. 1.

In this way the same analogue device (Σ-Δ Modulator) is used in all the parallel interleaving channels and the analogue impairments between channels no longer matters.

By using additional counters the sampling rate of the converter can be significantly increased.

3. Results of Verifying Simulation

For practical reasons simulation of very limited case has been presented. An example of only two interleaved counters was analyzed, but more counters can be added and their maximum number would be when they are interleaved by one clock pulse only. However for the converter resolution of e.g. 22 bits it would be the prohibitive number of 4194304 counters.

Using Microcap [11] circuit simulator, simple 1st order Σ-Δ Modulator action was simulated, using a slowly rising ramp voltage as input source. The output pulses of the modulator were recorded and stored in a file. Simulating counter action, the number of output pulses was counted during 64 clock pulses starting from zero time. It was equivalent to the production of 6 bits samples with 16 ms sampling interval. Again it is very low converter resolution but increasing it to e.g. 22 bits would increase dramatically simulation time. The decimal values of consecutive samples are presented in Table 1.

The samples were placed along the time axis as shown in Fig. 6a. The next set of samples was obtained again by counting the number of modulator output pulses with the same sampling interval, but starting 8 ms later. It was equivalent to the action of the second counter. The values of consecutive samples are presented in the Table 1. The samples were again place along the time axis as shown in Fig.6b.

The samples from both counters are taken sequentially as the output digital signal so that they can be placed along the same time axis; this results in doubling the sampling rate as shown in Fig.6c.

4. Conclusions

For practical reasons an example of only two interleaved counters was given above, with very low resolution of only 6 bits, but more counters can be added and their resolution increased by extending the counting time.

It is thus theoretically possible to obtain multi-bit samples with high sampling frequency which theoretically can equal the frequency of the Σ-Δ modulator clock.

The possibility of increasing the sampling frequency by adding interleaved counters can be used to increase the number of bits in the samples above the necessary limits.

It would be possible to use modulators of lower order. Contemporary Σ-Δ AD converters employed in acoustic devices use modulators of order as high as fifth to limit the appearance of idle tones caused by the periodic appearance of quantizing errors. It is well known that using a modulator of order higher than second causes the modulator circuit to become unstable and special techniques should be used to prevent this. By using modulators of lower order and increasing the number of bits in the samples above the necessary limits it is possible simply to reject LSB and eliminate totally the periodic components of quantising error which causes the problem of idle tones in acoustic devices.

Table 1. Number of pulses recorded by first and second counter

Time [ms]	0	8	16	24	32	40	48	56	64	72	80	88	96
Number of pulses Counter 1	42	-	45	-	51	-	57	-	62	-	66	-	-
Number of pulses Counter 2	-	43	-	48	-	52	-	58	-	62	-	67	-

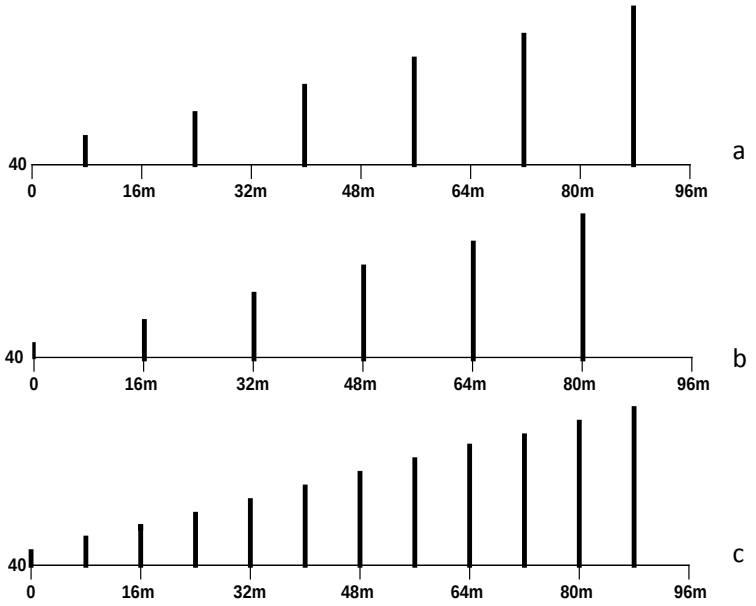

Figure 6. Samples of simulated action of Σ-Δ ADC with single Σ-Δ modulator and two time interleave counters

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