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A Novel Technique for Suppression of Corner Effect in Square Gate All Around Mosfet

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Abstract Square gate all around MOSFET is a promising device structure at present era of continued scaling due to their superior control over the short channel effects. However, it exhibits a undesirable effect known as corner effect which degrades the device performance by increasing the off state leakage current. In this work a new technique to suppress the corner effect has been proposed, modelled, simulated and its results have been compared with existing structure of square gate all around MOSFET.

Keywords Square Gate All Around MOSFET, Corner Effect, charge sharing, premature inversion

1. Introduction

The scaling of classical MOSFET is approaching its limit due to the short channel effects. So to overcome this problem multiple gate MOSFETs were introduced as a replacement of classical single gate MOSFET. As the numbers of gate increases multiple gate MOSFETs offer superior control over the channel, which helps to reduce short channel effects and leakage current[1]-[4]. According to the numbers of gates multiple gate MOSFETs are of various types, like Double gate MOSFET, Tri gate MOSFET, Gate all around(GAA) MOSFET (Cylindrical and Square). Among these multiple gate structures, Gate all around structure offers superior control over the channel due to its surrounding gate structure, which in turn reduces the short channel effect effectively[5]-[6]. Besides, GAA MOSFETs offer several advantages over single and other multiple gate MOSFETs like higher current drivability, mobility enhancement and so on. So due to these advantages, gate all around MOSFETs are considered as the excellent candidates for future CMOS integration.

Among the Gate all around structures, square gate all around MOSFET has higher current drive capability compared to cylindrical gate all around MOSFET. Despite these advantages, square gate all around MOSFET exhibits a very undesirable characteristic known as corner effect which occurs due to the electrostatic coupling of two adjacent gates at the corners. This effect degrades the device performance by increasing the off state leakage current. The corner effect can be minimized by rounding the corner regions [7]. But corner rounding is a delicate process. In this paper we propose a new method to suppress the corner effect occurs in square gate all around MOSFET.

Section 2 of the paper describes the corner effect of square gate all around MOSFET. Section 3 describes the newly proposed method for suppression of corner effect. The results of this newly proposed method has been discussed in section 4. Finally the section 5 carries the conclusion of this paper.

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2. Corner Effect in Square GAA Mosfets

Square gate all around MOSFET is types of multigate MOSFET where the gate warps around the four sides of the silicon channel[8]. The square gate all around MOSFET and its schematic description is shown in figure 1. The cross-section of the silicon surface has a square shape with width and height t_{si}. A layer of silicon dioxide (SiO_2) having thickness t_{OX}, is warped around the silicon surface which acts as an insulator between silicon surface and gate electrode. Since the gate electrode has wrapped the device in all directions, so at the corner regions as shown in figure 2 of the device due to the electrostatic coupling of two adjacent gates, charge sharing effect occurs that means at the corner region, the depletion charge is shared by two gates[9]. This causes reduction of threshold voltage at the corners. So the corners are turned on prior to the other parts of the device. So, premature inversions occur at the corners. This phenomenon is known as corner effect [10]-[11].

The threshold voltage of a square gate all around MOSFET is as follows

$$V_{th\_SQ} = \Phi_{ms} + 2\Phi_f + (|Q_b| / C_{OX\_Square}) \quad (1)$$

Since depletion charge has been shared by two adjacent gates at the corners so at the corner regions depletion regions charge density reaches maximum value, when the gate

contributes only half in the other parts. This causes reduction of surface potential. Mathematically it can be presented as,

$$V_{th\_corner} = \Phi_s + \Phi_{ms} + \frac{\frac{|Q_b|}{2}}{C_{ox\_Square}} \quad (2)$$

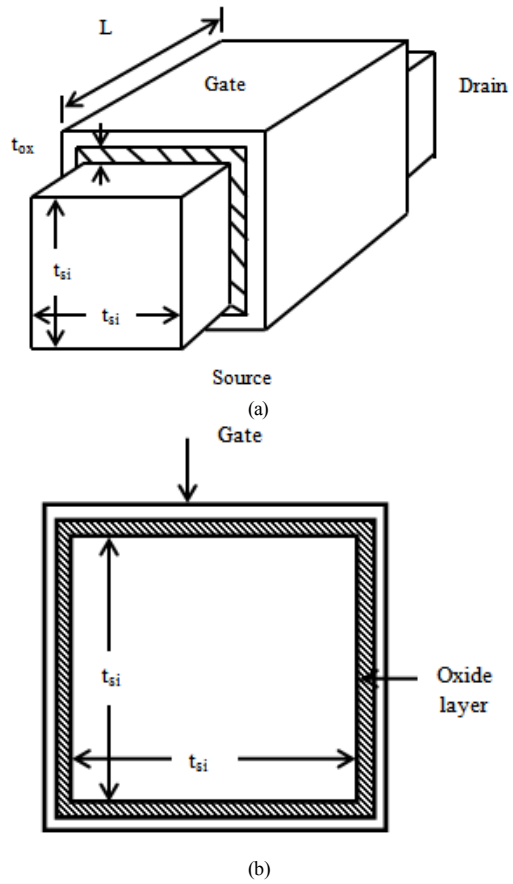

Figure 1. (a) Square gate all around MOSFET (b) Cross-section of square gate all around MOSFET

For square GAA MOSFET oxide capacitance is given by [12]

$$C_{OX\_Square} = \frac{5\varepsilon_{ox}}{4t_{si} \times \ln\left(1+\frac{5}{4}\times\frac{t_{ox}}{t_{si}}\right)}$$

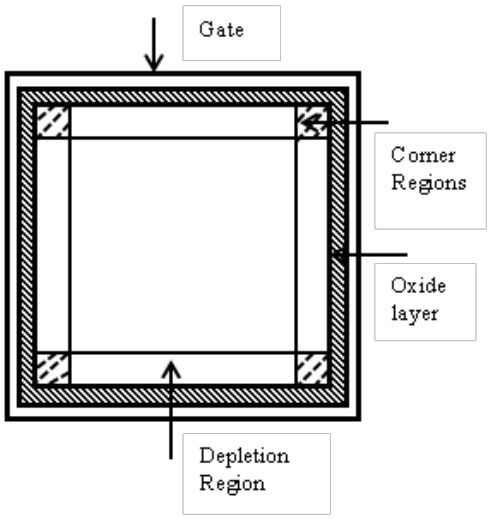

Figure 2. Square gate all around MOSFET with corner regions

At corner region charge contributed by each gate is

$$\frac{|Q_b|}{2} = \sqrt{2qN_a\,\varepsilon_{si}\,\Phi_s}$$

$$=> \frac{\sqrt{2qN_a\,\varepsilon_{si}\,2\Phi_f}}{2} = \sqrt{2qN_a\,\varepsilon_{si}\,\Phi_s}$$

$$=> \Phi_s = \frac{\Phi_f}{2} \quad (3)$$

So at the corner region threshold voltage is reduced to

$$V_{th\_corner} = \frac{\Phi_f}{2} + \Phi_{ms} + \frac{\frac{|Q_b|}{2}}{C_{ox\_Square}} \quad (4)$$

Figure 3 shows the variation of threshold voltage at the corners and other parts of a square gate all around MOSFET using n^+ polysilicon gate.This results increase of drain current at the corners. This corner current for linear region can be modelled as

$$I_{D\_corner\,(lin)} = \mu C_{OX\_SQ}\frac{W_1}{L}\left[(V_{GS} - V_{th\_corner})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (5)$$

$$W_1 = \text{width of the channel at the corners} = 8\times X_{dm} \quad (6)$$

For saturation region

$$I_{D\_corner\,(sat)} = \mu C_{OX\_SQ}\frac{W_1}{2L}(V_{GS} - V_{th\_corner})^2 \quad (7)$$

And current at other parts of the channel is

For linear region

$$I_{D\_surface\,(lin)} = \mu C_{OX\_SQ}\frac{W_2}{L}\left[(V_{GS} - V_{th\_Square})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (8)$$

For saturation region

$$I_{D\_surface\,(sat)} = \mu C_{OX\_SQ}\frac{W_2}{2L}(V_{GS} - V_{th\_Square})^2 \quad (9)$$

$$W2 = \text{width of the channel at the other parts of the channel} = (4\times tsi) - W1 \quad (10)$$

So the total drain current of a square gate all around MOSFET for linear region

$$I_{D\_total(lin)} = \mu C_{OX\_Square}\frac{W_1}{L}\left[(V_{GS} - V_{th\_corner})V_{DS} - \frac{V_{DS}^2}{2}\right] + \mu C_{OX\_Square}\frac{W_2}{L}\left[(V_{GS} - V_{th\_Square})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (11)$$

For saturation region

$$I_{D\_total(sat)} = \mu C_{OX\_Square}\frac{W_1}{2L}(V_{GS} - V_{th\_corner})^2 + \mu C_{OX\_Square}\frac{W_2}{2L}(V_{GS} - V_{th\_Square})^2 \quad (12)$$

Figure 4 shows the variation of current at corners and other parts of the channel. Since current at the corners more than other parts of the channel so it degrades device performance.

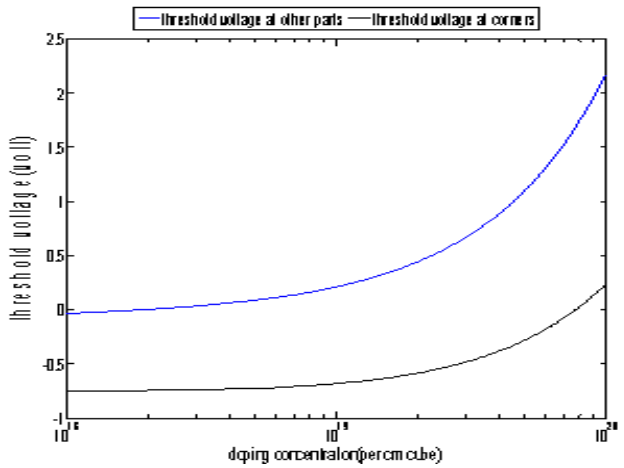

Figure 3. Variation of threshold voltage at corners and other parts of the device

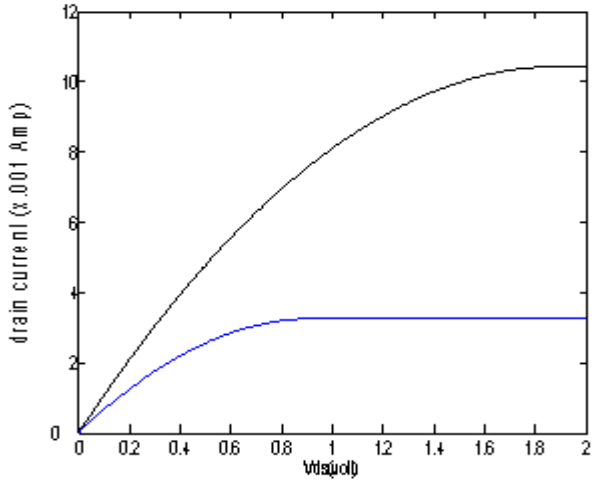

Figure 4. Variation of drain current at corners and other parts of the channel

3. A Novel Technique for Suppression of Corner Effect

The main reason behind the corner effect is charge sharing at corners. To overcome this problem in this work a new structure of square gate all around MOSFET has been proposed. This is known as " Square gate all around MOSFET with lateral gate underlap". In this structure instead of applying the gate in all directions, four gates are given to the four sides of the device with reduced gate width i.e the width is reduced from both the ends of the gate in each four sides of the device. Figure 5 shows the structure of a square gate all around MOSFET with lateral gate underlap. The width of the each gate is W and the thickness of the silicon surface is t_{si}. The width of the underlap region on both ends of each gate is W'. This structure can be better explained with the aid of a parallel plate capacitor with unequal plate area. Suppose the gate material is considered as the upper plate and silicon surface is lower plate. Length of the upper plate is L and its width is W, while the width of the lower plate is W+2*w'* as shown in figure 6. Distance between two plates is t_{OX} and permittivity is ε_{OX}. So the capacitance at the region where both plates are of equal dimensions is

$$C_{OX} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{13}$$

For unequal plate region there exists an additional width at the lower plate w' on each side. The electric field (E) of the equal plate portion is uniform. But in unequal plate portion it is not uniform. In both sides of the additional width, as the width increases the electric field decreases as $E\cos\theta_1$, $E\cos\theta_2$

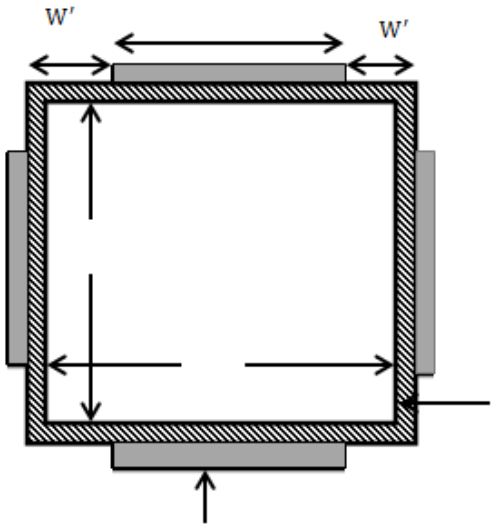

Figure 5. Square gate all around MOSFET with gate underlap

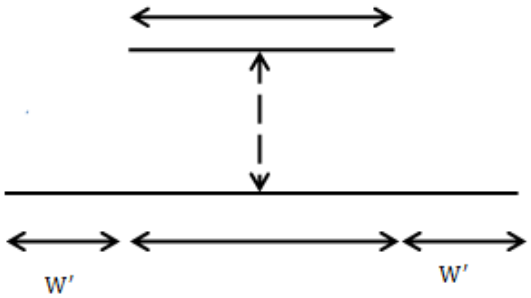

Figure 6. Parallel plate capacitor with unequal plate dimension

and so on and so as capacitance. This variation of electric field is shown in figure 7. So the total electric field in unequal plate portion is

$$E' = E\cos\theta_1 + E\cos\theta_2 + = \sum_{i=1}^{n} E\cos\theta_i \tag{14}$$

Now, total capacitance of the unequal plate portion is

$$C' = \frac{|Q|}{|V|} \tag{15}$$

According to Gauss law,

$$\begin{aligned} |Q'| &= \oint_s \varepsilon_{ox} E' ds \\ &= \oint_s \varepsilon_{ox} E\cos\theta_i ds \\ &= \varepsilon_{ox} E\cos\theta_i W' L \end{aligned} \tag{16}$$

So,

$$\begin{aligned} C' &= \frac{\varepsilon_{ox} E \cos\theta_i w' L}{E t_{ox}} \\ &= \frac{\varepsilon_{ox} \cos\theta_i w' L}{t_{ox}} \end{aligned} \tag{17}$$

Now for per unit area of the unequal parallel plate section capacitance is

$$C = \frac{\varepsilon_{ox} \cos\theta_i}{t_{ox}} \quad (18)$$

Where θ_i is the maximum range up to which electric field can generate in unequal parallel plate section of the MOS and it can calculate as

$$\theta_i = \tan^{-1}\left(\frac{w'}{t_{ox}}\right) \quad (19)$$

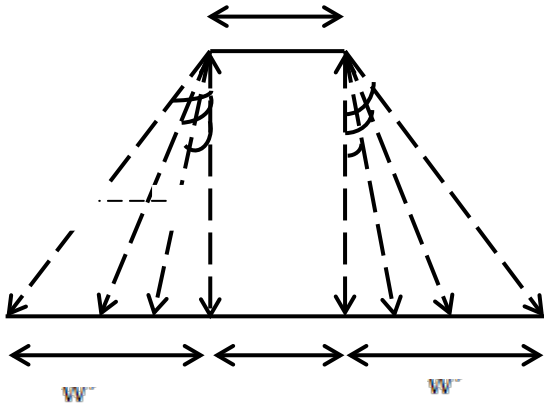

Figure 7. Variation of electric field in unequal parallel plate portion

The capacitance of the unequal parallel plate section of the device is less than the capacitance of the equal parallel plate. To minimize the corner effect up to highest possible level, the capacitance of unequal parallel plate section is considered as half of the capacitance of the equal parallel plate portion. Mathematically,

$$C = \frac{1}{2} C_{OX} \quad (20)$$

$$\Rightarrow \frac{\varepsilon_{ox} \cos\theta_i}{t_{ox}} = \frac{1}{2} \times \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\Rightarrow \cos\theta_i = \frac{1}{2} \Rightarrow \tan^{-1}\frac{w'}{t_{ox}} = 60°$$

$$\Rightarrow \frac{w'}{t_{ox}} = 1.73 \Rightarrow w' = 1.73 \times t_{OX} \quad (21)$$

So to minimize corner effect, underlaped region should be 1.73 times of the oxide thickness. Which means that the amount of width which is removed from both the ends of all four gates in four sides of the device is equal to 1.73 times of t_{OX}.

Since width of all the four gates are reduced, so when a positive voltage is applied to all four gates a depletion region will create at the beneath of each gate. But due to the fringing electric field, a smaller depletion region will generate in gate underlap region. So the depletion charge of this depletion region is less than the depletion region generated beneath the gate. Here it is assumed that the depletion charge of gate underlap region is the half of the depletion charge of actual depletion region. So,

$$Q_{b\_unerlap} = \frac{1}{2} Q_b \quad (22)$$

Since the it is contributed by both the sides, so overall charge density becomes Q_b only.

The threshold voltage at the non underlap gate region is

$$V_{th} = 2|\phi_f| + \Phi_{ms} + \frac{|Q_b|}{C_{ox}} \quad (23)$$

Where, $C_{OX} = \frac{\varepsilon_{ox}}{t_{ox}}$ (F/cm^2)

In case of square gate all around MOSFET with gate underlap structure, at the underlap region capacitance and depletion charge is reduced to half of the capacitance and depletion charge of non underlap region. The threshold voltage at the unerlap region is

$$V_{th\_underlap} = 2|\phi_f| + \Phi_{ms} + \frac{\frac{|Q_b|}{2}}{\frac{C_{ox}}{2}}$$

$$= 2|\phi_f| + \Phi_{ms} + \frac{|Q_b|}{C_{ox}} = V_{th} \quad (24)$$

So threshold voltage at gate underlap region is same as non underlap region. So in square gate all around MOSFET with gate underlap structure, threshold voltage at corner region remain same as the threshold voltage at other parts of the device. This results in corner current and total current of the device. The modified corner current is

For linear region

$$I_{D\_corner(underlap)} = \mu C \frac{W_1}{L}[(V_{GS} - V_{th\_unerlap})V_{DS} - \frac{V_{DS}^2}{2}] \quad (25)$$

For saturation region

$$I_{D\_corner(underlap)} = \mu C \frac{W_1}{2L} (V_{GS} - V_{th\_unerlap})^2 \quad (26)$$

C = capacitance at gate underlap regions

From equation 20

$$C = \frac{1}{2} C_{OX}$$

And from equation 24

$$V_{th\_unerlap} = V_{th}$$

So the equation 25 can be written as

For linear region

$$I_{D\_corner(underlap)} = \mu\frac{C_{ox}}{2} \frac{W_1}{L}[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}] \quad (27)$$

For saturation region

$$I_{D\_corner(underlap)} = \mu\frac{C_{ox}}{2} \frac{W_1}{2L} (V_{GS} - V_{th})^2 \quad (28)$$

The total current of the device at linear region

$$I_{D\_total(underlap)} = \mu C\frac{W_1}{L}[(V_{GS} - V_{th\_underlap})V_{DS} - \frac{V_{DS}^2}{2}] +$$

$$\mu C_{OX} \frac{W_2}{L}[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}] \quad (29)$$

$$= \mu\frac{C_{ox}}{2} \frac{W_1}{L}[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2_2}] +$$

$$\mu C_{OX} \frac{W_2}{L}[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}}{2}] \quad (30)$$

And for saturation regions

$$I_{D\_total(underlap)} = \mu C \frac{W_1}{2L}[(V_{GS} - V_{th\_underlap})^2] +$$

$$\mu C_{OX} \frac{W_2}{2L}[(V_{GS} - V_{th})^2]$$

$$= \mu\frac{C_{ox}}{2} \frac{W_1}{2L}[(V_{GS} - V_{th})^2] + \mu C_{OX} \frac{W_2}{2L}[(V_{GS} - V_{th})^2] \quad (31)$$

So from equation 30 and 31 it is clear that the corner current of a square gate all around MOSFET with gate underlap structure is lower than the corner current of a normal square gate MOSFET. So using gate underlap technique corner current can be minimized. But simultaneously it reduces the total current driving capability of the device.

4. Results and Discussion

To minimize the corner effect a new structure of square gate all around gate MOSFET has been discussed in section 3. In this structure four gates are given to the four sides of the device with reduced gate width. The physics of this new structure is similar to a parallel plate capacitor with unequal plate dimensions. In parallel plate capacitor the capacitance is uniform at the region where both plates are of equal dimensions due. But electric field is not uniform in the region where both the plates are of not equal dimensions. In this region electric field is reduced which in turn reduces the capacitance. Figure 8 shows the plot of variation of capacitance in gate underlap region. The capacitance decreases in gate underlap region and it becomes half at the corner position.

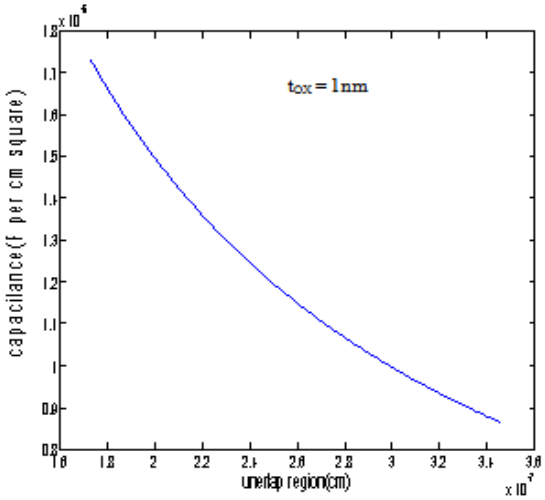

Figure 8. Variation of capacitance at gate underlap region

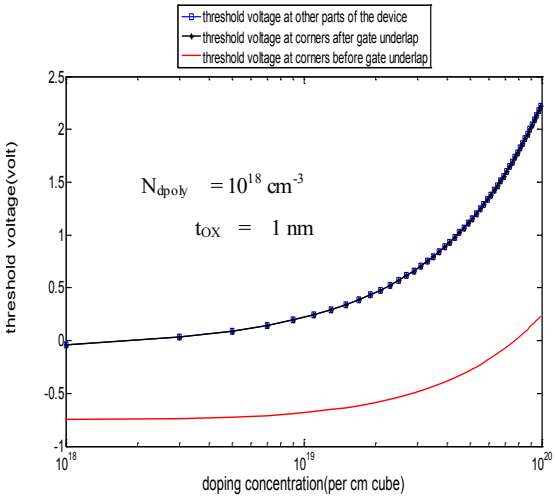

Figure 9. Variation of threshold voltage at corner positions and other parts of the device with and without using gate underlap technique

Figure 9 shows the variation of threshold voltage with doping concentration at corner regions and the other parts of the device for a square gate all around MOSFET with and without gate underlap. It is clearly shown that for a square gate all around MOSFET without gate underalp the threshold voltage at the corner regions is lower than the other parts. But for a square gate all around MOSFET with gate underlap, threshold voltage is equal at corner positions and other parts which can be seen from figure 9.

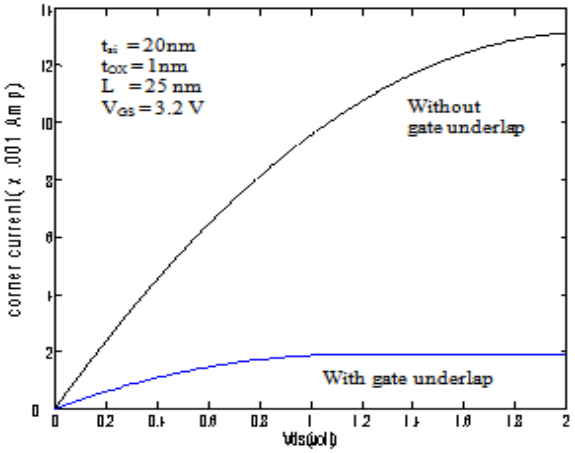

Figure 10. Reduction of corner current with gate underlap

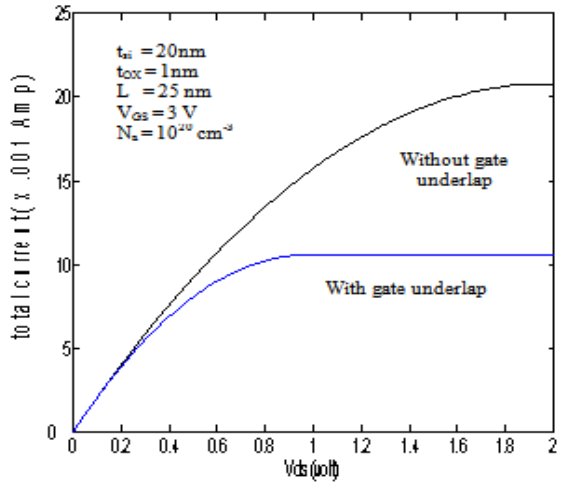

Figure 11. Reduction of total current with gate underlap

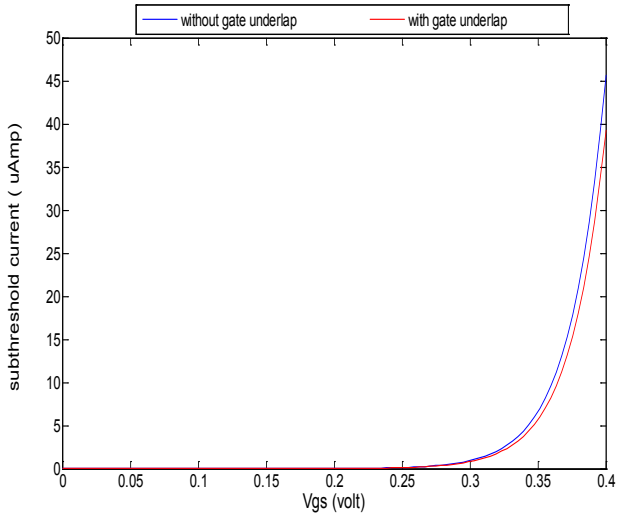

Figure 12. Reuduction of subthreshold leakage current with gate underlap

Figure 10 shows corner current- V_{ds} plot for a square gate all around MOSFET with and without gate underlap. Since for a gate underlap structure threshold voltage is equal at

corner positions and other parts, so current at corner regions remain same as other parts of the device. So using gate underlap structure corner current can be minimized, which is clearly shown in figure 10.

Figure 11 shows total current- V_{ds} plot for a square gate all around MOSFET with and without using gate unerlap. Since corner current is reduced using gate underlap (from figure 10), hence it reduces the total current of the device.

Figure 12 shows the variation of subthreshold leakage current for a square gate all around MOSFET with and without using gate underlap. From this figure it can be observed that subthreshold leakage current is lower in case of gate underlap structure.

5. Conclusions

This paper studies the corner effect of a square gate all around MOSFET which occurs due to charge sharing effect between two adjacent gates. This effect degrades the device performance by increasing the current at corners leading to premature inversion. To minimize this effect, in this paper a new structure of square gate all around MOSFET known as "square gate all around MOSFET with gate underlap" has been proposed and the same has been modeled and simulated. Also this model has been compared with conventional square gate all around MOSFET. From this comparison it is clear that the threshold voltage and hence the current at the corner regions of this new structure is same as the threshold voltage and current at other parts of the device. It also reduces the subthreshold leakage current. But simultaneously this structure reduces the total current of the device. Although this structure reduces the total current driving capability of the device still it protects the device from unwanted corner effect.

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