

Analyze of DGMOS Tunneling Current through Nanoscale Gate Oxide

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Abstract The DGMOSFET (Double Gate Metal Oxide Semiconductor Field Effect Transistor) is considered as the most promising device in nanometer scale [1, 2, 3]. Indeed, it presents an excellent control of the short channel effects [4]. We can cite the Drain Induced Barrier Lowering (DIBL), Subthreshold current, Subthreshold voltage slope (S), lower leakage current (I_{off}) and better 'On' Current. However, the gate direct tunnelling current is the major components of leakage currents in DG MOSFET and has been shown to become one mechanism of the degradation of device performances at ultra-thin oxide (around 1.5nm). We present in this paper an analyze and a control of the gate tunnelling leakage current. This analyse is based on an own software which consist to solve self consistly Poisson (1) and Schrödinger (2) equations for undoped (or lightly doped) symmetric double gate (DG) MOSFET. Quantum effects and short channel effects (SCE) due to nanometer sizes, hence are taken into account. This approach allows an accurate analyse of the manometer device. The results show that the current tunnelling does set an ultimate scaling limit.

Keywords DGMOS, Nanometer, Self-consistent, Tunnelling effect, High k

1. Introduction

Recent advancement in ultimate scaling of CMOS technology have allowed microelectronics industry to fabricate CMOS transistors with gate lengths below 10 nm. The decrease in the size of microelectronic components leads to a reduction of cost and in the performance of improvement components. However, this leads to the occurrence of adverse effects. To minimize them, it is interesting to look at new architectures of transistors, such as double gate MOSFET that is considered now as a promising alternative [3]. As promising candidate, a great researches effort has been devoted to multi-gate nanodevices, and especially doubles gate devices (DGMOSFET).

The principal of a double gate MOSFET is to control the silicon channel very efficiently with a very small channel width [4]. It consists to apply a gate contact to both sides of the channel. This concept helps to eliminate short channel effects and leads to higher current compared to the conventional TMOS. Source to drain tunnelling is an illustration of a full pseudo-2D aspect, and has been shown to become one mechanism of the degradation of device performances at ultra-thin oxide (1.5nm). However, the gate direct tunnelling current is the major components of leakage

in DG MOSFET [1, 2]. The principle computations are based on the self-consistent solution of Poisson's (1) and Schrodinger equation (2) [5], gives a valuable insight into the underlying physics of the tunnelling mechanism. We solve the obtained system of differential equations using finite differences method and Newton-Raphson algorithm.

Results show that a higher gate tunnelling current is obtained in the case of lower oxide thickness. In order to minimize it, high-k materials has been considered and investigated.

In this paper, we will analyse the tunnelling direct current and its effects on the performances devices.

2. Device Structure and Mathematical Model

The reduction of devices dimensions to nanometer sizes reveals of quantum nature phenomena. For this, numerical calculations are based on self-consistent codes, which consist to couple Poisson (1) and Schrödinger (2) equations. This is necessary when the oxide thickness is decrease and the thickness channel takes values close to the wavelength of the electrons.

$$\frac{d^2V(x,y)}{dx^2} + \frac{d^2V(x,y)}{dy^2} = -\frac{\rho(x,y)}{\epsilon_0\epsilon_r} \quad (1)$$

$$-\frac{\hbar^2}{2m^*} \frac{d^2\psi(y)}{dy^2} + qV(y)\psi(y) = E\psi(y) \quad (2)$$

Where, ϵ_r is the permittivity of the silicon, $\psi(y)$ is the

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wave function, E the quantized energy and $V(y)$ the electrostatic potential. The total charge density, ρ , present in a P-type semiconductor is given by the following equation:

$$\rho(x, y) = -q[p(x, y) - n(x, y) + N_D^+(x, y) - N_A^-(x, y)] \quad (3)$$

Where, q is the elementary charge, N_D^+ and N_A^- are the ionized impurity concentration and $n(x, y)$ and $p(x, y)$ are the carriers concentrations.

The potential profile in the tow- dimensional simulations domains obeys the Poisson equation. Schrodinger one is solved assuming an effective mass approximation for each 'x' across the device.

The main computations give a valuable insight into the underlying physics of the tunnelling mechanism. We solve the obtained system equations using finite differences method and Newton-Raphson algorithm [6]. The considered structure and its corresponding mesh are presented on figure 1.

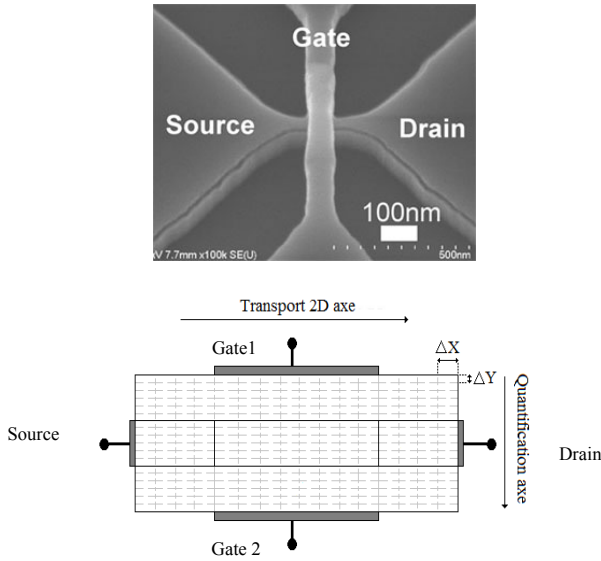


Figure 1. a) SEM image (Scanning Electron Microscopy) of DGMOS. (Source: AIST) b) Considered mesh for the Double Gate MOS transistor

The gate tunnel current in dependence on the bias voltage, semiconductor layer thickness as well as the gate oxide layer thickness has been carefully investigated.

The gate current (tunnel) is calculated according to the following expression [7]:

$$J_G = \sum \sum f_{i,j} Q_{i,j} T_{TD}(E_{i,j}) \quad (4)$$

Where $T_{TD}(E_{i,j})$ is the transparency Tunnel, $f_{i,j}$ is the trial impact frequency of electrons hitting the appropriate oxide barrier plane and $Q_{i,j}$ is the total charge.

2.1. Transparency Tunnel

To calculate the Transparency Tunnel analytically, we use WKB approximation (Wentzel - Kramers - Brillouin). The transparency tunnel is expressed as [7]:

$$T_{TD}(E_{i,j}) = \exp \left[\frac{8\pi T_{ox} \sqrt{2m_{ox}}}{3q} \frac{V_{ox}}{h} ((q\phi_{ox} - E_{i,j})^{3/2} - (q\phi_{ox} - qV_{ox} - E_{i,j})^{3/2}) \right] \quad (5)$$

Where T_{ox} is the oxide thickness, m_{ox} is the electron mass in the oxide, ϕ_{ox} is the barrier height of electrons, $E_{i,j}$ is the potential energy in the oxide / semiconductor interface and V_{ox} is the potential in the oxide.

2.2. Frequency of Impact

We suppose that the trial impact frequency of electrons f is limited by the motion in the semiconductor body for tunnelling from both the substrate to the gate and from the gate to the substrate [7]:

The frequency of impact can be written as:

$$f_{i,j} = \frac{q\epsilon_{ox} V_{ox}}{4T_{ox} \epsilon_s} \frac{1}{\sqrt{m_i E_{i,j} / 3}} \quad (6)$$

Where: ϵ_{ox} and ϵ_s are the permittivity of the oxide and the permittivity of the semiconductor.

2.3. Frequency of Impact

The total charge is expressed by:

$$Q_{i,j} = \frac{qg_i m_i K_B T}{\pi h^2} \ln \left[1 + \exp \frac{E_{F_n} - E_{i,j}}{K_B T} \right] \quad (7)$$

In all calculation, we assume that interface SiO₂/Si is parallel to the <100> plane. In this case, six equivalent minima of the bulk silicon conduction band split into two sets of sub-bands (fig 2).

Indeed, there are two ladders of the energy levels: $j=1$ or 2 , corresponding to two possible effective masses: $m_1 = m_l = 0.91m_0$ and $m_2 = m_t = m_0$ for electrons in six valleys of the Silicon conduction band and the degeneration factors for all this cases are $g_1=2$, $g_2=4$ [8].

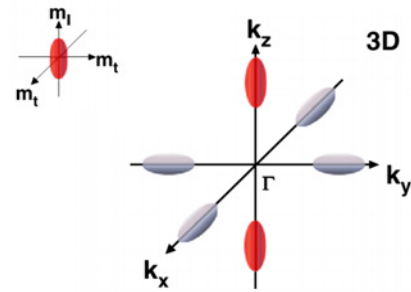


Figure 2. Iso-energy surfaces of the bottom of the conduction band of silicon

The tunnelling current I_G equals to the density of electrons J_G multiply by the surface.

$$I_G = J_G \cdot S \quad (8)$$

In our structure there are two tunnel currents I_{G1} and I_{G2} . The total tunnelling current is the sum of them:

$$I_G = I_{G1} + I_{G2} \quad (9)$$

3. Results

First of all, the figure 3 permit to validate our calculations with 2D numerical simulations performed with Atlas software.

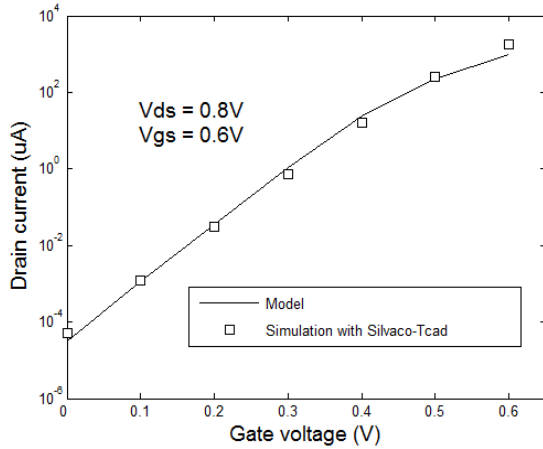


Figure 3. Comparison between the program and the SILVACO-TCAD software

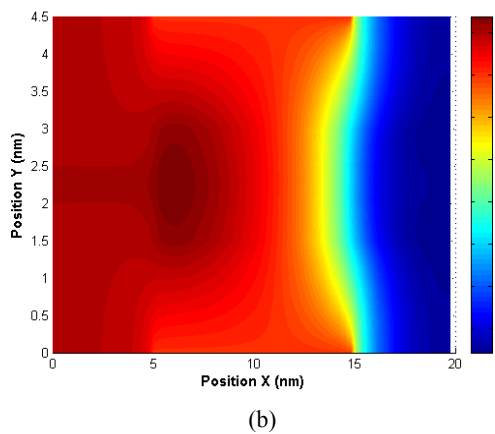
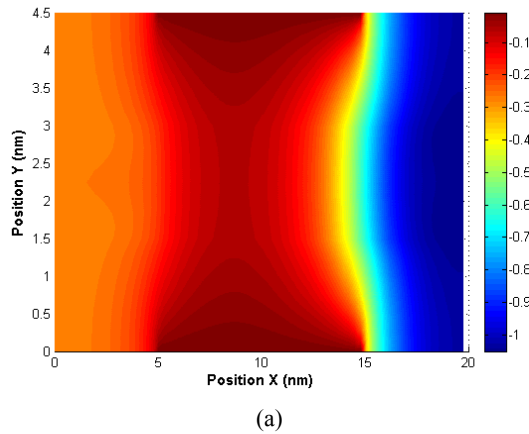


Figure 4. Distribution potential energy for $V_{ds}=0.8V$ and: (a) $V_{gs}=0.2V$, (b) $V_{gs}=0.6V$

The Figures 4 and 5 represents the potential energy and the density of electrons DGMOS transistor for different gate voltages V_{gs} and for a drain-source voltage equal 0.8 V. The

considered structure (figure 1-a) has a channel lengths equals 10 nm and source/drain length $L_{sd} = 5nm$. These later regions are doped with $N_D = 10^{20} cm^{-3}$ but the channel is intrinsic type. We can observe clearly the potential energy barrier between the source and the channel region.

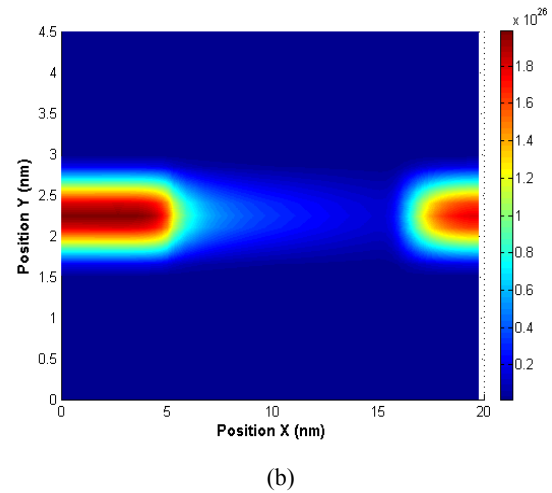
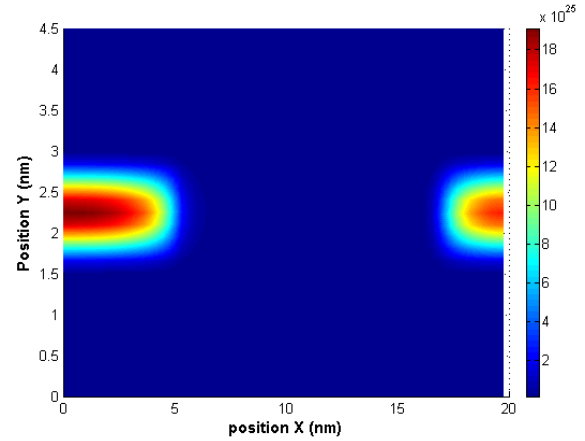


Figure 5. Distribution of the electron density for $V_{ds}=0.8V$ and: (a) $V_{gs}=0.2V$, (b) $V_{gs}=0.6V$

We observe that the distribution of the potential energy between the source and drain regions. Therefore, the potential barrier between the source and the channel is variable.

Indeed, for a low gate voltage, the potential barrier prohibits the passage of electrons from source to drain. However, for voltage values larger, the potential barrier decreases and electrons can pass from the source to the drain electrodes.

The distribution of the electron density on the DGMOS structure is shown on Figure 5, for different gate voltages: $V_{gs} = 0.2 V, 0.6V$ and $V_{ds} = 0.8V$.

We can clearly note the passage of electrons from the source to the drain regions. So the electron channel which connects the two source-drain junctions is created.

On figure 6, we observe the drain current versus the drain voltage and the gate one. The tunnelling effect is

characterized by the passage of the carriers through the oxide. The direct tunnelling current is the dominant type of conduction in ultra-thin oxide MOS structures (<3nm) [9, 10]. To model it, the Wentzel - Kramers - Brillouin (WKB) approximations have been largely used [7, 11]. It depends exponentially on the electric field across the oxide (equa. 4).

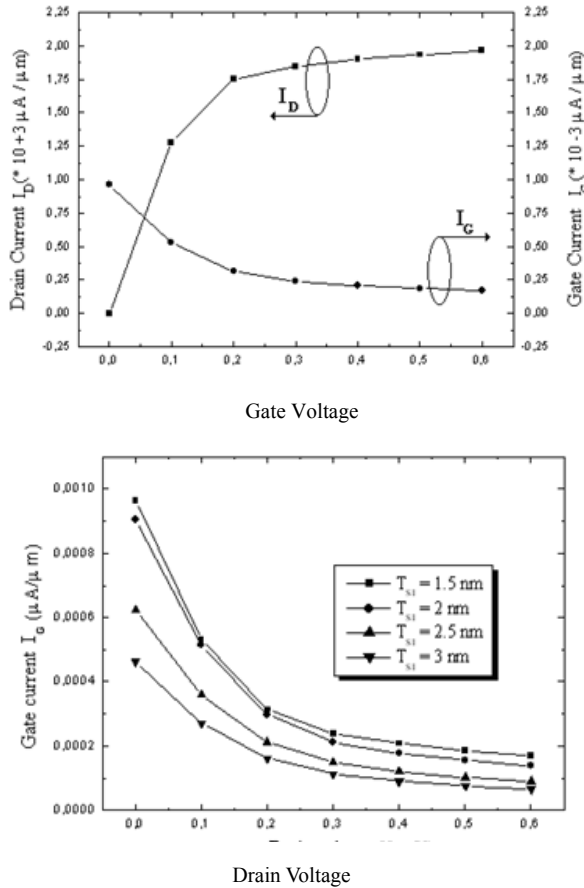


Figure 6. a) Gate voltage dependences of the drain and the gate current, b) Gate current vs. Drain voltage for different silicon thickness

It is clear that the gate current increases dramatically when the oxide thicknesses decreases. In fact, in this case, the electrons transit rapidly the silicon region. The transit time is then very short. Such, electrons can then reaches the gate region [1]. Moreover, the reduction of the gate oxide thickness results in an increase of the electric field across the oxide.

Figure 7 shows some significant results with considering the Hafnium (HfO_2) and the Zirconium (ZrO_2) as oxide gate. The dielectric constant in both cases is evaluated as 20 and 25 respectively. The silicon oxide thickness is $T_{SiO_2} = 1.5$ nm and the corresponding Equivalent Oxide Thickness EOT is $EOT_{HfO_2} = 7.7$ nm and $EOT_{ZrO_2} = 9.6$ nm. The results show that the tunnelling current is an ultimate scaling and confirm that an alternative to improve the DGMOSFET performances is the considering of high-k technology [12].

In all calculations, we have considered metal gate electrodes. The type of this electrode has been introduced in order to overcome the depletions effects of the doped

polysilicon electrode gate, namely gate electrode depletion.

Figure 7 represents the leakage current versus the gate metal work function. In order to reduce this later, metal gate electrodes will require work function that can be turned to a desired value.

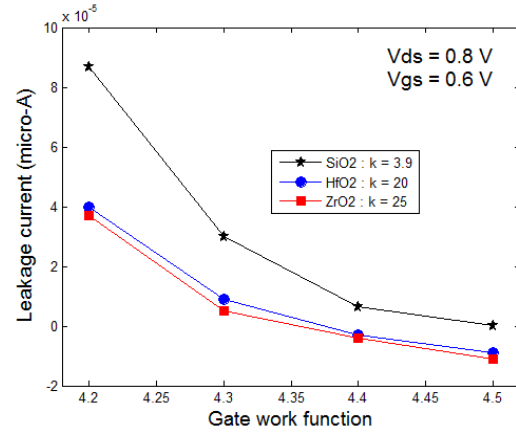


Figure 7. Leakage current vs. gate work function for different gate oxides

4. Conclusions

A 2D self consistent model which takes into account the quantum mechanical effects and the short channel effects such as threshold voltage, sub-threshold voltage slope, leakage current and DIBL has been considered with appropriate boundary conditions.

We have especially pointed off the leakage current in this paper. This rigorous approach is able to bridge advanced computational methods for nano-scale DGMOS. Since tunneling current and gate work function limit the device performances, the results of this paper provide useful indications for different technological options for the realization of the DG MOSFET.

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