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Tremendous Opportunities to Improve DGMOSFET by High Mobility Materials Channel

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Abstract There has been significant effort in simulations to benchmark the performance of nanoscale DGMOSFET transistors using high mobility channel. Different architectures, substrate orientations and strain effects are investigated by several methods and approach for Ge PMOS. However, replacement of Si channel by Ge requires several critical issues to be addressed in Ge PMOS technology. A comparaison of Ge and Si as channel in the DGMOSFET has been carried out.

Keywords SOI-DGMOSFET, CMOS, Quantum effects, Quantum-drift-diffusion, Local Fermi level, High mobility

1. Introduction

Starting to attain adequate drive current for the highly scaled MOSFETs (below the 22nm technological node [1]), high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed due to a smaller effective mass in Ge can potentially lead to higher carrier mobility and drive currents in Ge MOSFETs than in Si MOSFETs. Ge is particularly well suited for p-type devices, thanks to its high hole mobility which is about four times greater than that of silicon, as well as some processing related issues, such as dopant solubility and Fermi level pinning at the valence band. Ge MOSFETs with different gate dielectrics including HfO_2 [2], ZrO_2 [3], have been demonstrated.

There has been significant effort in simulations to benchmark the performance of nanoscale Ge transistors. Different architectures, substrate orientations and strain effects are investigated by several research groups for Ge NMOS and PMOS. However, replacement of Si channel by Ge requires several critical issues to be addressed in Ge MOS technology. High quality gate dielectric for surface passivation, low parasitic source/drain resistance and performance improvement in Ge NMOS are among the major challenges in realizing Ge CMOS.

In this work we use the nextnano code to simulate a DG-MOSFET with high-k gate dielectric [17] and Ge channel. This simulation tool is based on the self-consistent solution of the Schrödinger, Poisson and current equations [4, 5]. The coupled Poisson-Schrödinger system is solved by an approximate quantum charge density, which is employed inside of Poisson's equation in order to estimate the dependence of the density on the potential through Schrödinger's equation. Using this estimator the coupling between both equations is much decreased and rapid convergence is achieved.

The electronic structure is calculated within a single-band or multiband k .p envelope function approximation. The included model for the carrier transport is a Wentzel–Kramer–Brillouin (WKB)- type approach also known as quantum-drift-diffusion (QDD) method, where the carriers are locally in equilibrium, charactized by a local Fermi level [6, 7].

The main aim of this paper is to provide an insight by replacing Silicon in the channel by Ge using different dielectric constants. A comparaison of Ge has been made with both HfO_2, ZrO_2 and Si with SiO_2. Current-voltage (I-V) curves are demonstrated by varying the channel doping concentration.

The outline of the paper is as follows. Section II describes device structure. Section III presents some theoretical aspects. Section IV shows the simulation results using Quantum-drift-diffusion method. Section V concludes the paper.

2. Structure and Simulation Details

Fig. 1 shows the structure of simulated device SOI DGMOSFET. The device parameters is summarised in table 1. This symmetric structure is characterized by p-type doped channel using Si and Ge channel of 6nm width. This channel is embedded between two heavily n-doped source and drain regions of length 10 nm that are connected to source and drain contacts. The junctions are assumed to be abrupt. The polysilicon gates are separated from the Si and

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the Ge channels by an oxide layer and the power supply voltage V_{DD} is 0.7V. In order to highlight the performance of device at 22nm technological node and by using different channel doping, we have carried out the calculation by varying different dielectrics ZrO_2 and HfO_2 while maintaining the same channel width (6 nm) and oxide thickness (1.1nm).

The channel doping (NA) is changed to maintain the constant Vth which is tabulated in Table 1.

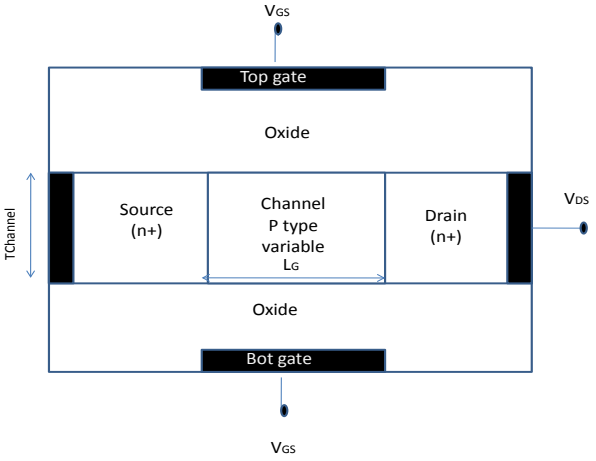

Figure 1. Symmetrical DG-MOSFET considered in this work

Table 1. Device parameters taken for design

Parameters	Value
Gate Length	18nm
Gate oxide thickness	1.1nm
Source/Drain Doping	10^{20}cm^{-3}
Channel doping	0.1×10^{15},cm^{-3},1×10^{15} cm^{-3}, 10×10^{15} cm^{-3}

3. Calculation Method

The drift-diffusion model is widely used for simulation of carrier transport in semiconductors this model had been taken for simulating the electronic structure within Nextnano3 [8, 9], and is defined by the basic semiconductor equations. Current density for electrons is given by:

The Poisson equation:

$$\nabla^2\psi = \frac{q}{\varepsilon}\cdot(n-p-c) \tag{1}$$

The current continuity equation for electrons and holes:

$$\begin{aligned}\nabla\vec{J}_n - q\cdot\frac{\partial n}{\partial t} &= q\cdot R\\ \nabla\vec{J}_p - q\cdot\frac{\partial p}{\partial t} &= -q\cdot R\end{aligned} \tag{2}$$

The current relations for electrons and holes:

$$\begin{aligned}\vec{J}_n &= q\cdot n\cdot\mu_n\cdot\vec{E}_n + q\cdot D_n\cdot\nabla_n\\ \vec{J}_p &= q\cdot p\cdot\mu_p\cdot\vec{E}_p - q\cdot D_p\cdot\nabla_p\end{aligned} \tag{3}$$

The charge density is calculated for a given applied voltage by assuming the carriers to be in a local equilibrium that is characterized by energy-band dependent local quasi-Fermi levels $E_{Fc}(x)$ for charge carriers of type c (i.e. in the simplest case, one for holes and one for electrons),

$$n_c(x) = \sum_i \left|\psi_{ic}(x)\right|^2 f\left(\frac{E_{Fc}(x)-E_{ic}}{k_BT}\right) \tag{4}$$

These local quasi-Fermi levels are determined by global current conservation $\nabla\cdot j_c = 0$, where the current is assumed to be given by the semi-classical relation :

$$j_c(x) = \mu_c n_c(x)\nabla E_{Fc}(x) \tag{5}$$

The carrier wave functions ψ_{ic} and energies E_{ic} are calculated by solving the multiband Schrodinger-Poisson equation [4].

The EOT used in this work is that obtained by classical Electrostatic theory in planar devices where:

$$EOT = \frac{k_{SiO2}}{k_{high-k}}T_{high-k} \tag{6}$$

The SiO_2, HfO_2 and ZrO_2 permittivities are 3.9,21.2 and 25 respectively.

Due to the increase of the gate dielectric thickness, the leakage current J_g by tunnel effect is then significantly reduced. Indeed, this one decrease exponentially with the gate dielectric thickness

$$J_g = \frac{A}{T^2_{high-k}}\,exp\left[-2T_{high-k}\sqrt{\frac{2m^*q}{\hbar^2}\left(\Phi_B - \frac{V_{high-k}}{2}\right)}\right] \tag{7}$$

with:

A: constant m^*: carriers effective mass *q:* electron charge

$\hbar$: Planck constant Φ_B : unevenness between the level of the Si conduction band and high k material. V_{high-k} : Loss of voltage through the dielectric.

For long channel devices, the sub-threshold slope, which is the gate voltage excursion required to increase the drain current by one decade in the weak inversion regime, results from the voltage sharing between the gate dielectrics and the depletion region of the transistor. It is expressed as:

$$S = \frac{KT}{q}\ln(10)\left[1+\frac{Cdep}{Cox}\right], \tag{8}$$

where k is the Boltzmann constant, q the elementary charge, T the temperature, $Cdep$ and Cox the depletion and the gate oxide capacitances, respectively.

4. Results

The off-state current is influenced by several parameters such as channel physical dimensions, source/drain junction depth, thickness of gate oxide, channel/surface doping profile and supply voltage (V_{dd}) [17]. To overcome these impact, we explore the possibility of using Ge as a channel material in p-type MOSFETs with Schottky barrier (SB) contacts. As the Ge concentration is increased, drain current is also increased because of the enhanced mobility.

Fig2 shows the I_{DS} versus V_{GS} curves at constant V_{DS} of 0.7V for different channel materials for EOT=1.1nm, HfO_2

and ZrO_2 gate dielectrics with Ge shows higher drain current but it requires lower threshold voltage which results short channel effects (SCEs) take dominance, therefore germanium material channel are preferable for given threshold voltage as shown in the inset of Fig2.

OFF current varies sharply with permittivity with Ge channel. It was revealed that the drain-current for the Ge channel DG MOSFETs was tremendously improved when compared to the Si channel. Also the OFF current for undoped channel raise as the permittivity decrease and its more higher than doped channel.

The off-state current I_{off} at V_{GS}=0V When applying HfO_2 is 0.169A/m In the case of ZrO_2 dielectric and Ge channel, the off-state current I_{off} at V_{GS}=0V is 0.121A/m. and is 1,09A/m in the case of SiO_2 with Si channel. The HfO_2I_{off} and ZrO_2 I_{off} is much less than SiO_2. With increase in channel doping Off-state current get increses. (Table 2).

The threshold voltage from I_{DS}–V_{GS} characteristics at V_{DS} = 0.7V. is increasing with the increment of permittivity using Ge channel (Fig.3).

The threshold voltage lowering is increasing continuously with the channel Doping Fig.3 shows the variation of threshold with different doping levels [16].

HfO_2 and ZrO_2 gate dielectrics with Ge at 10×10^{15} level doping show higher drain current but it require lower threshold voltage thus it is possible to increase subthreshold effects. So we can have desired value of the threshold voltage by varying the channel doping. But high channel doping cannot be done as it leads to gate induced drain leakage. The suitable value of channel doping is 10^{15} and value of threshold voltage at this doping level are106.8 mV for the ZrO_2 which is optimum value of threshold voltage for the gate length of 18 nm. Therefore, one using Silicon with SiO_2, it will be higher (Figure 4).

Table 2. Variation of I_{off} with channel doping

Channel Doping conc. (cm^{-3})	I_{off} for HfO_2 A/m	I_{off} for ZrO_2 A/m	I_{off} for SiO_2 A/m
Witout doping	0,492	0.313	3,8705
0.1×10^{15}	0,126	0.111	1,009
1×10^{15}	0,169	0.121	1,091
10×10^{15}	0, 475	0.305	1,1089

Table 3. Variation of SS with channel doping

Channel Doping conc. (cm^{-3})	SS for HfO_2 mV/decade^{-1}	SS for ZrO_2	SS for SiO_2
Witout doping	78.98	75.8	188.4
0.1×10^{15}	65.05	55.48	180.21
1×10^{15}	67.16	59.7	183.1
10×10^{15}	69.68	62.2	186.4

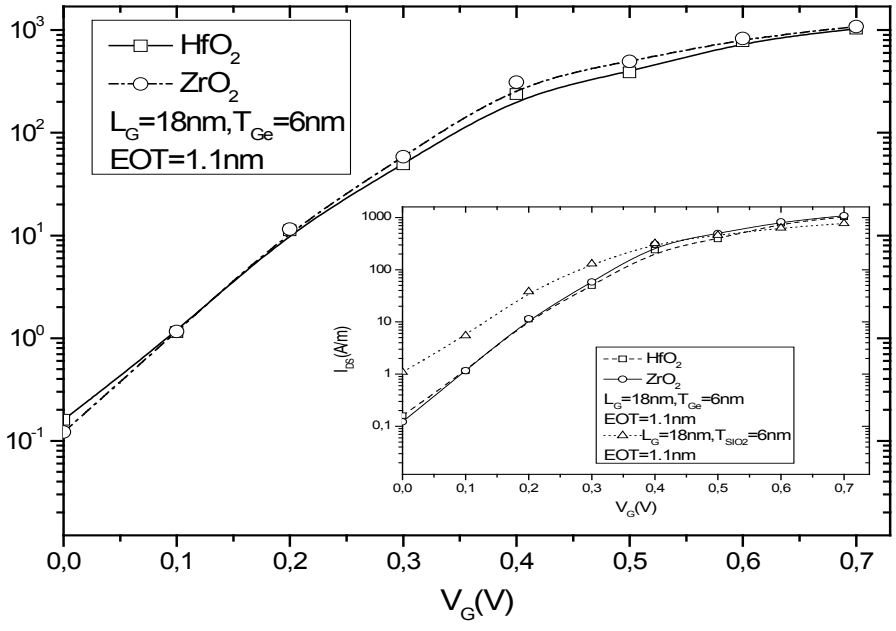

Figure 2. I_{DS} versus V_{GS} characteristics of DGMOSFETs for $HfO_2$and ZrO_2

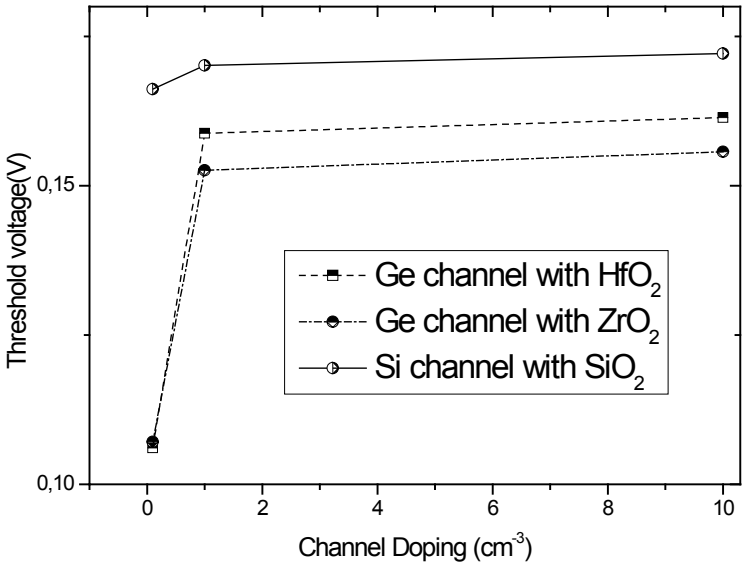

Figure 3. Threshold voltage versus Channel doping

For the various results obtained using simulation approach, lower value of subthreshold swing is desirable so lightly doped channel devices with high permittivity are preferred over doped and undoped channel devices. As we increase the channel doping, subthreshold swing increases linearly as shown in Table 4.

Figure 5 shows the subthreshold region of MOSFETs which has a significant high gain due to exponential behavior of the drain current thus gives rise to higher transconductance generation factor (Gm/I_D) in the subthreshold regime [10, 11]. gm and Gm/I_D are directly dependent on the drain current. So, the structure having Ge channel gives rise to higher values of transconductance, maximum value of transconductance and maximum value of output conductance are outlined in table4.By comparing these values while dopping channel varying from 0.1×10^{15} to 10×10^{15} the Tansconductance (G_m) is decreased by 5.4% for SiO_2 and 24.7% for ZrO_2 And 27,9% for HfO_2. G_d is increased by 28.8% for HfO_2 and 10. 3% forZrO_2 and 35.5%f or SiO_2.we can see the variation G_m and G_d in Fig.6 (plots G_m versus channel doping (in the inset Gd versus channel doping)). Higher transconductance means gate has more control over the charge in the channel (Table 4).

From Fig.5 it's clear that tas the V_{gs} increases the G_m / I_d decreases In this figure, the maximum performance can be obtained in ZrO_2 G_m / I_d ratio by comparing with HfO_2 and SiO_2.

ON-State current, decides the driving capability of the device. It is defined as drain to source current when $Vgs=V_{dd}$ and $Vds= V_{dd}$. Fig.7 demonstrates the I_d-V_d characteristics for Si and Ge channel DG MOSFETs. Here, the current in Ge channels is increased compared to Si channel, due to the enhanced mobility. It means the mobility of charge carrier in Ge channel is higher due to which they give higher Ion. saturation occurs around 0.28 volts to 0.41 volts for all the channel materials. Si and SiO_2 gets saturated at almost at the same voltage of 0.28 volts Ge with ZrO_2 and HfO_2 get saturated at 0.41V. have higher saturation current around 935A/m On the whole this figure indicates that Ge using high permittivity have more current density as compared to Si, which is highly desired for channel material.

Table 4 given shows the drive current variation for different doping levels. We can see the decrease of I_{ON} as channel doping increase. The drain current is dependent on the mobility of carriers which is controlled by the doping concentrations. When the channel doping is kept high which results a lower drain current then the device having higher NA.

Ge MOSFETs with different gate dielectrics including HfO_2 [12, 13], ZrO_2 [13, 14, 15], the high permittivity increases I_{on} and decrease I_{off}. More ever the I_{on} and I_{off} for HfO_2 and ZrO_2 dielectric are summarized in Tables 2 and 5.

The I_{on}/I_{off} current ratio represents the power consumption of a device. As we increase the channel doping drive current reduces almost linearly, but off state current decreases exponentially. This leads to increase in I_{on}/I_{off} ratio very sharply as shown in Figure 8.

Figure. 9 shows gate direct tunneling current as function of channel doping for $V_{DS}=V_{DD}=0.7V$, $V_{GS}=0.7V$. The gate direct tunneling current takes a minimum value in the case of silicium and maximum value in the case of ZrO_2. So If we increase channel doping and permittivity one parameter get improved while other get worse.

The improvement in electron density has been investigated in terms of channel doping in Fig.10; this figure shows a slice through the middle of the device ($y=T_{Si}/2$=constant) for different channel doping under a drain bias of 0.7V. The electron Density increases and it is highest in the middle of the channel region and is practically zero at the Si/SiO_2; Ge/ZrO_2 and Ge/HfO_2 interfaces. For gate bias voltage equal to 0.7V as shown in the figure of electron density, the Ge channel electron density with HfO_2 and ZrO_2 significantly differs from Si channel using SiO_2 and takes its maximum when reducing the channel doping.

Table 4. Variation of G_m and G_d with channel doping

Channel Doping conc. (cm^{-3})	G_m for HfO_2 (S)	G_m for ZrO_2 (S)	G_m for SiO_2 (S)	G_d for HfO_2 (S)	G_d for ZrO_2 (S)	G_d for SiO_2 (S)
0.1×10^{15}	2378,7	2391,26	1750,59	1056.2	910	1033.17
1×10^{15}	1901.4	1905,2	1697,21	1096	985.89	1016
10×10^{15}	1714.11	1799.2	1655,9	1361.59	1004	1400

Table 5. Variation of I_{ON} with channel doping

Channel Doping conc. (cm^{-3})	I_{ON} for HfO_2 Ge channel A/m	I_{ON} for ZrO_2 Ge channel A/m	I_{ON} for SiO_2 Si channel A/m
Witout doping	1018,2	1025,9	612.1
0.1×10^{15}	1039,14	1078,86	734.72
1×10^{15}	1035,11	1071,59	772,21
10×10^{15}	1028,11	1070,14	771.38

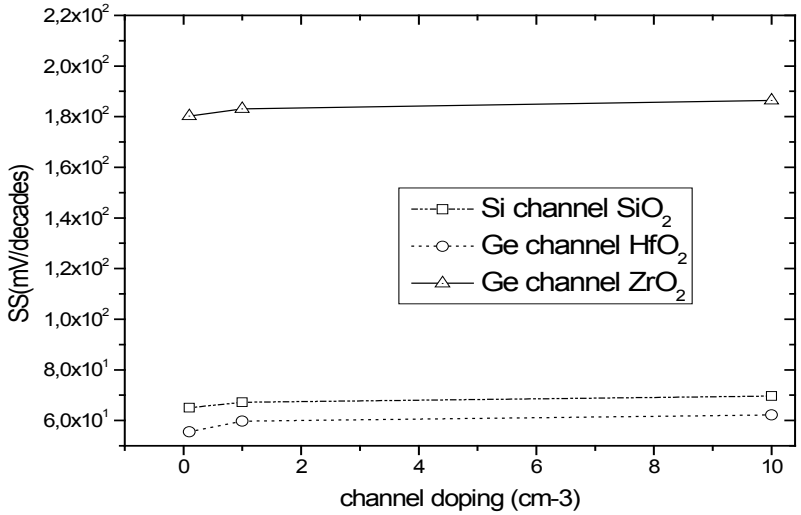

Figure 4. Subthreshold swing versus Channel doping

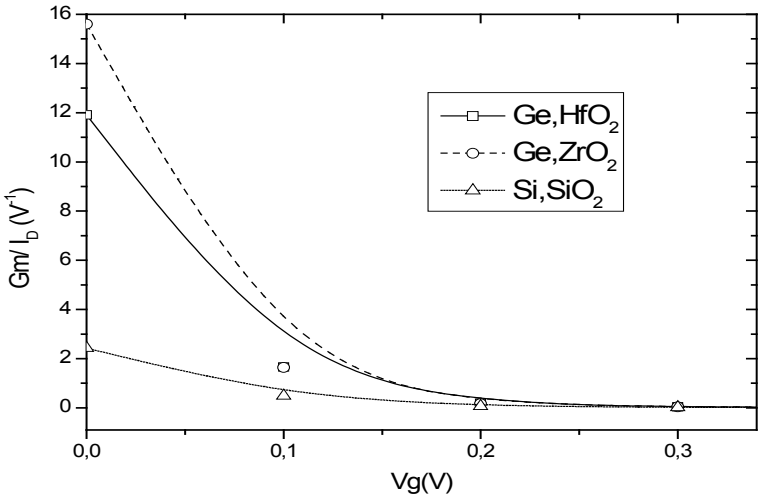

Figure 5. G_m/ I_{DS} versus V_g for $HfO_2$and ZrO_2 with Ge channel and SiO_2 with Si channel

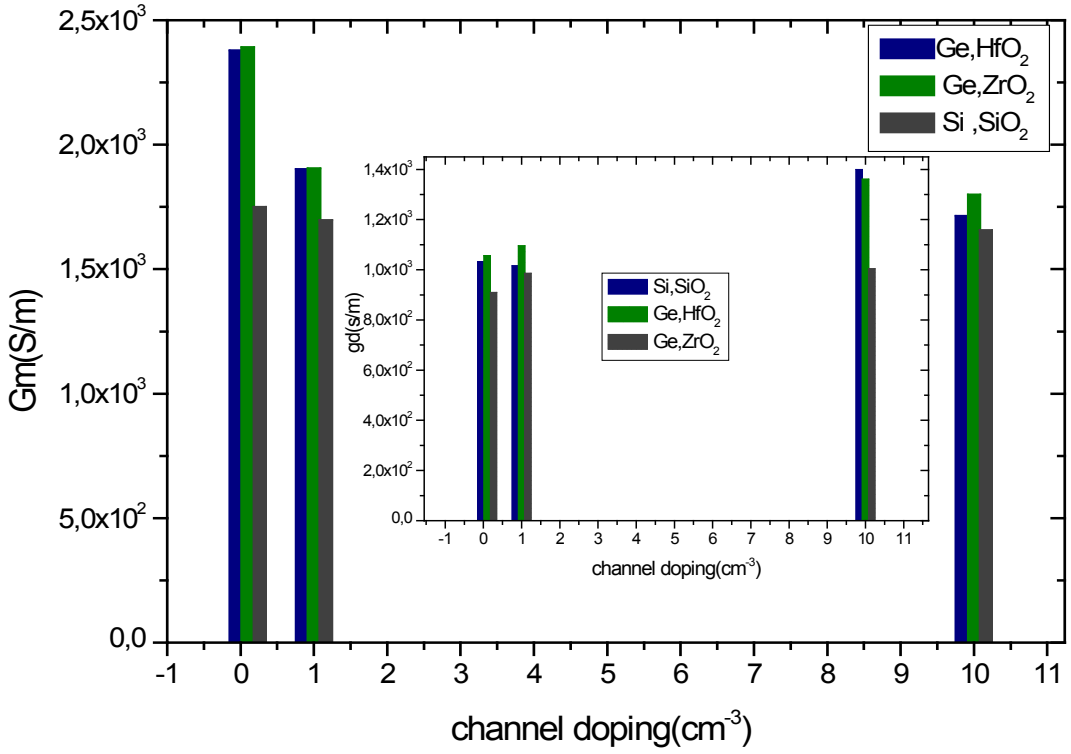

Figure 6. Gm and Gd versus Channel doping

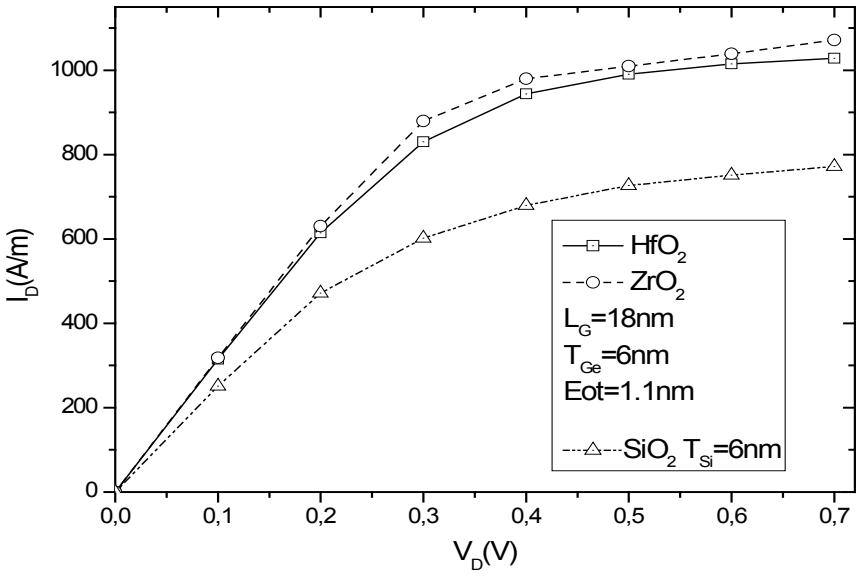

Figure 7. I_{DS} versus V_{DS} characteristics of DGMOSFETs for $HfO_2$and ZrO_2 with Ge channel and SiO_2 with Si channel

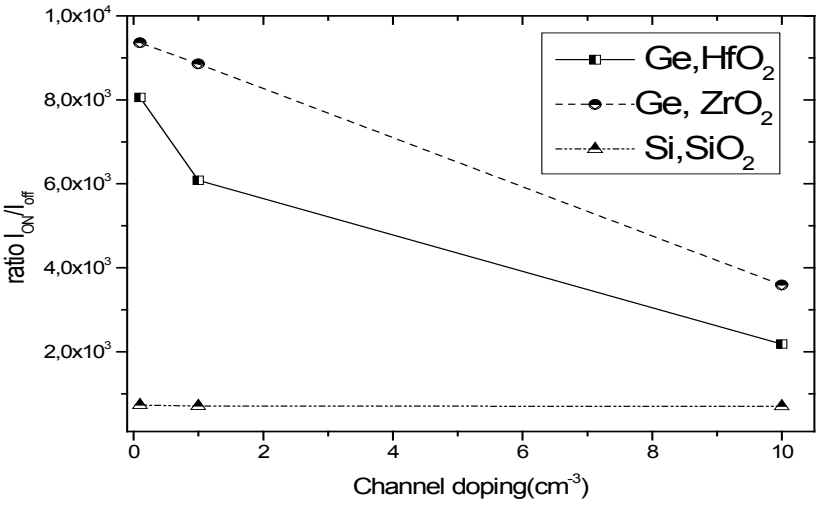

Figure 8. Ratio I_{on}/I_{off}versus channel doping

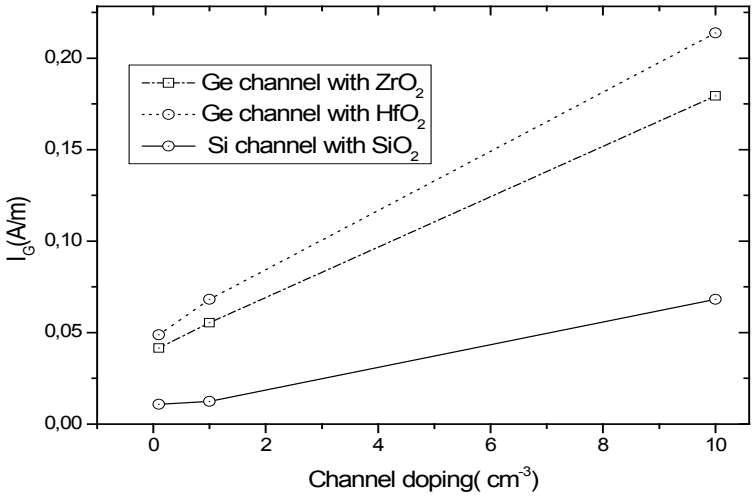

Figure 9. Gate current $I_g$versus channel doping

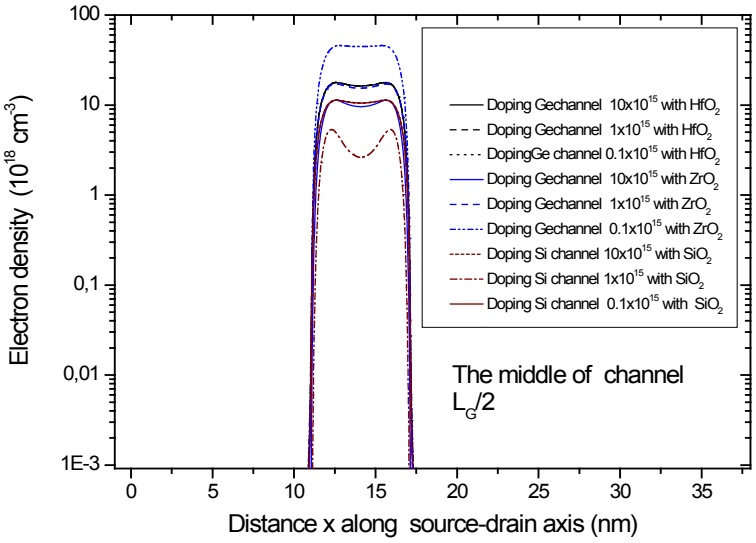

Figure 10. Electron density versus channel doping

5. Conclusions

In comparison to Si as a channel material, Ge is more desirable. Our calculations predict that Ge channel devices Using the high permitivity has a good control of gate and the drain current increases with the increase of permittivity. We also cannot use high doping because mobility degradation of carrier takes place in the channel region. The increase of permitivity with Ge channel when channel doping was raised improve somme parameters like subthreshold swing and highest output conductance at different values of oxide thickness. Our calculated and simulated results show that the optimized value of channel doping is 1×10^{15} using ZrO_2.

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